Letter

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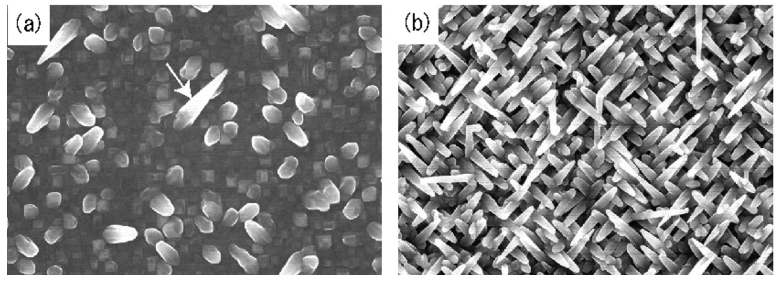

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Vertical Epitaxial Wire-on-Wire Growth of Ge/Si on Si(100) Substrate

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ABSTRACT

Vertically aligned epitaxial Ge/Si heterostructure nanowire arrays on Si(100) substrates were prepared by a two-step chemical vapor deposition method in anodic aluminum oxide templates. *n*-Butylgermane vapor was employed as new safer precursor for Ge nanowire growth instead of germane. First a Si nanowire was grown by the vapor liquid solid growth mechanism using Au as catalyst and silane. The second step was the growth of Ge nanowires on top of the Si nanowires. The method presented will allow preparing epitaxially grown vertical heterostructure nanowires consisting of multiple materials on an arbitrary substrate avoiding undesired lateral growth.

In order to combine epitaxial semiconductor nanowires grown via a bottom-up process such as the VLS (vapor−liquid−solid) technique with conventional Si micro/nanoelectronics, the control of the growth direction of the nanowires is one of the most important issues. Usually, homoepitaxial Si nanowires grow along ⟨111⟩, ⟨110⟩, and ⟨112⟩ directions, and heteroepitaxial Ge nanowires on bare Si(100) substrate grow along ⟨111⟩ and ⟨110⟩, respectively.[1−5] From an application viewpoint involving semiconductor nanowires for FET devices, Ge nanowires have promising electrical characteristics due to their high electron mobility compared to Si nanowires. Therefore, control of the growth direction of Ge nanowires is quite important for the realization of vertical Ge nanowire FETs and has been studied by several groups.[2,4,5] Typically, in order to produce Ge nanowires using the VLS mechanism, GeH_4 is employed as the Ge source gas, despite its toxicity and highly hazardous nature.[2,4,5] The lack of an inherently safe growth process is known as one of the major limitations of commercial Ge production using chemical vapor deposition (CVD) processes.[6] Searching for a safer Ge source gas instead of GeH_4 is, therefore, important and highly desirable for Ge nanowire growth via VLS. In addition, a Ge/Si buffer structure on a Si substrate would be interesting for the integration of III−V semiconductor nanowire lasers with Si-based logic circuits. Due to the special one-dimensional character of nanowires, a Ge/Si buffer structure could work as a relaxed buffer layer for the growth of InGaAs/GaAs on Si substrate, without any dislocations, if the nanowire diameter is below the critical radius.[7]

Several reports on $Si_{1-x}Ge_x$/Si[8,9] nanowires and on Si/Ge[10] nanowires grown by the VLS mechanism have already been published. Moreover, nonepitaxial growth of $Si_{1-x}Ge_x$/Si heterostructure nanowires in anodic aluminum oxide (AAO) templates, which have nanoscale pore arrays aligned in one direction, was performed using a so-called template-direct-growth method by Lew et al.[9] The authors showed that the template growth method allowed to synthesize single crystal heterostructure nanowires via the VLS growth mechanism in a template, and the diameter of the nanowires could be controlled by the size of the AAO pores.[9] The observed longitudinal crystal orientations of these nanowires were ⟨111⟩, ⟨110⟩, and ⟨112⟩, which are the same as the preferred growth directions of the nanowires without a template. However, ⟨100⟩ nanowires, which would be important to combine vertical nanowire transistors with conventional microelectronics on bare (100) substrates, had not been observed. Recently, we reported the growth of epitaxial Si[100] nanowires on Si(100) substrate using AAO as a template to grow the epitaxial nanowires.[11−13] In the present study, we first prepared epitaxially grown Ge nanowires on Si(100) substrate using a less toxic Ge source gas. Using the growth parameters obtained from these growth experiments, subsequently epitaxial vertical Ge nanowires on homoepitaxially grown Si[100] nanowires on Si(100) substrates using AAO templates were grown.

We employed *n*-butylgermane (ABCR GmbH & Co. KG, $C_4H_{12}Ge$, 95%) as source gas to grow Ge nanowires in consideration of the following properties: substantially less

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hazardous and less toxic compared to GeH_4, easy to handle liquid with acceptable vapor pressures at room temperature, and good thermal stability. Au was used as catalyst for VLS growth of Ge nanowires on bare Si substrates and Ge/Si heterostructure nanowires in AAO templates. In the case of bare Si substrates, 1 nm thick Au was deposited onto the H-terminated Si(100) substrate by thermal evaporation in ultrahigh vacuum (UHV) conditions. A *n*-butylgermane liquid source as a Ge precursor was installed at the UHV-CVD system. The background pressure in the UHV system was lower than 10^{-9} mbar, and the growth pressure after filling in the *n*-butylgermane vapor was 4.6×10^{-1} mbar. The Ge CVD growth was carried out for 4 min at temperatures from 370 to 500 °C.

For the preparation of Ge/Si nanowires (Ge nanowire on top of Si nanowire) in the template, an AAO membrane with 60 nm pores on a Si(100) substrate was prepared by the same procedure as in the previous report.[11] The catalyst Au was deposited at each pore bottom on the Si surface by electroless deposition. Growth of the Si nanowires was carried out at a temperature of 400 °C for 10 min using a mixture of 5% silane and 95% Ar as a precursor gas. After growth of the Si part, the Si precursor gas was stopped, while the growth chamber was evacuated down to UHV condition again. The setting of the heater was changed for a nominal temperature of 370 °C. The temperature of the substrate was decreased to a small value far below the eutectic temperature of about 360 °C by increasing the distance between substrate and heater from 1 mm to 10 cm. Subsequently, *n*-butylgermane vapor was introduced into the chamber, up to a pressure of 2.6×10^{-1} mbar. The substrate was moved to approach the heater, and growth continued for 7 min.

Scanning electron microscopy (SEM) observation was performed using a Jeol 6701F. Cross-sectioned samples were prepared by mechanical thinning and ion milling, as transmission electron microscopy (TEM) specimens. TEM observations utilized both a Philips CM 20 with EDX and a Jeol JEM 4010 which are 200 and 400 keV instruments capable of obtaining a point resolution of about 0.3 and 0.16 nm, and the spot diameter of energy dispersive X-ray (EDX) measurements was about 50 nm.

Figure 1 shows top view SEM images after the Ge CVD process on bare Si(100) substrate. Here, vertical and horizontal directions of the picture are adjusted to ⟨110⟩ directions. The nanowires have a bright contrast in this image, while they tend to grow along several growth directions. All nanowires grew along either the ⟨111⟩ or the ⟨110⟩ direction, which was defined by the crystallographic orientation of the Si substrate. This result suggests that the nanowires were grown epitaxially on bare Si(100) substrates, and *n*-butylgermane can be used as precursor to grow Ge nanowires. Au-catalyzed Ge nanowire growth using *n*-butylgermane as precursor was limited to the temperature range from ~370 to 470 °C. Figure 1a shows the Ge nanowires grown near the highest limitation temperature. Most of the deposited Ge formed three-dimensional block shape structures on the substrate, although several nanowires with strong tapering, which appeared corn shaped, could be

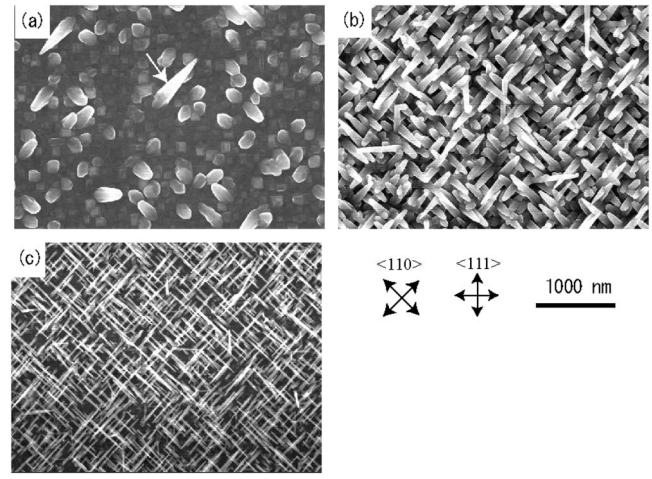

Figure 1. Top view SEM images of Ge nanowires grown on bare Si(100) substrate. The samples were grown at (a) 450, (b) 400, and (c) 370 °C for a duration of 4 min in *n*-butylgermane at a pressure of 4.6×10^{-1} mbar, respectively. The white arrow in (a) points out a strongly tapered wire. Crossed arrows indicate crystal orientations of the Si substrate projected on its (100) surface.

observed. This three-dimensional growth of Ge can be explained by uncatalyzed decomposition of *n*-butylgermane occurring on the Si or Ge surface. Only a few Au particles worked as a catalyst at this temperature, and Ge nanowires with strong tapering indicated by white arrows in Figure 1a can be seen. Uncatalyzed deposition on the side walls of the nanowires, which was about 0.2 times slower than the catalyzed wire growth rate, induced the tapering. Although such an uncatalyzed deposition could not be avoided completely, tapering of the nanowires was reduced using lower growth temperatures as shown in Figure 1c.

After CVD growth, macroscopic information, in particular the surface color of the samples, gave nanoscopic information. The samples grown at relatively high temperatures, higher than 480 °C, showed metallic color, this suggests a nearly flat surface of the samples due to uncatalyzed deposition. At a growth temperature of 450 °C, during growing the nanowires, the surface got rough and showed a smoky gray color after the growth. In the temperature range from 450 to 370 °C, the color also changes from smoky gray to brown, which depends on the diameter of the nanowires. The average diameter of Ge nanowires in the brown color region was about 30 nm.

Previous studies about Ge nanowire growth on Si(100) substrate showed that the nanowires with diameter larger than 20 nm tend to grow along ⟨111⟩ directions.[2,4,5] However, ⟨110⟩ growth is dominant in Figure 1a−c. The average diameter of the nanowires estimated from Figure 1c was about 20 nm. Mainly there are two approaches to explain preferred growth directions of nanowires; some models are based on the free energy at the interface between liquid catalyst and solid nanowire,[1,14] others look to kinetic effects related to growth speed.[3,15] The free energy theory predicts that larger diameter nanowires tend to grow along ⟨111⟩ directions, and smaller diameters tend to grow along ⟨110⟩ growth directions. The crossover diameter was 20 nm for Ge nanowires[2] and 30 nm for Si nanowires,[1] respectively.

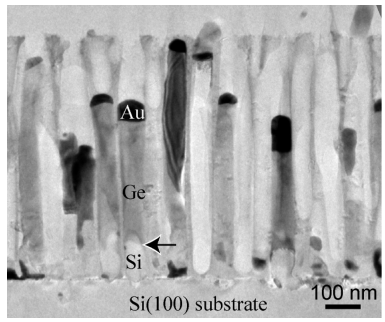

Figure 2. Cross-sectional TEM image of Ge/Si nanowire in the AAO template. The arrow indicates a interface between Ge and Si.

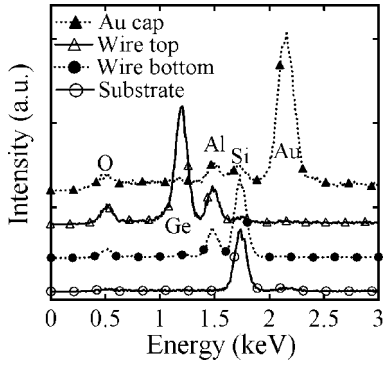

Figure 3. EDX spectra taken from Au cap (solid triangles), upper part of the nanowire higher than the interface indicated in Figure 2 by arrow (outlined triangles), bottom part of the nanowire lower than the interface (solid circles), and the Si substrate (outlined circles) with energy range from 0.3 to 3 keV. The diameter of the electron beam was about 50 nm.

On the other hand, the kinetic effect on nanowire growth, which appears in the case of high growth rates, shows always ⟨110⟩ direction regardless of its diameter. In the present study, the growth rate estimated from Figure 3c was relatively high at 185 nm/min. Therefore, it seems that the kinetic effect was dominant in the growth behavior of these Ge nanowires. In fact, the majority of growth directions of Ge nanowires grown using a low growth rate (94 nm/min) by lower *n*-butylgermane partial pressure (2.6×10^{-1} mbar) were changed to the ⟨111⟩ direction.

Although epitaxial nanowires were grown, the control of growth orientation in order to obtain perpendicular nanowires was not possible on bare Si(100) substrates. We, therefore, grew the nanowires in AAO templates to force the growth direction of the wires along the AAO pore direction perpendicular to the substrate. Figure 2 shows a cross sectional TEM image of the Ge/Si nanowires in the 650 nm thick AAO template. Each nanowire has an Au cap with strong dark contrast on the top, and the wires were grown perpendicular to the Si(100) substrate. They fit to the pores with a diameter of about 80 nm, and tapered growth was not observed. Along the wire direction, there are two segments, which can be distinguished by material contrast in the nanowire. The interface between the two segments is indicated with an arrow in Figure 2. These segments were recognized as Ge (upper part) and Si (bottom part) by EDX with an energy range from 0.3 to 3 keV shown in Figure 3.

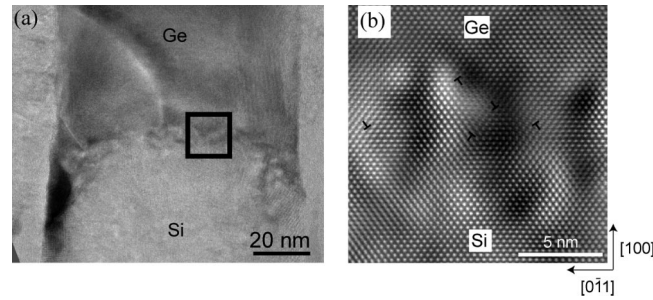

Figure 4. (a) HR-TEM image of Ge/Si nanowire at the interface between Ge and Si. (b) FFT-filtered image of the interface shown in panel a. "T" symbols indicate positions and orientations of dislocations. The terminated lattice planes are of ⟨111⟩ type. The lattice misfit between Si and Ge is relaxed by dislocations with usual symbol orientation; one dislocation of each dislocation loop has an upside down symbol orientation.

Although we expected a small amount of Si contained in the Ge parts, the Si peak was not observed within our limit of resolution. O and Al peaks originating from the AAO template were observed in the spectra except for the substrate part, due to the growth of the nanowires inside the pores of an AAO template. The advantage of template growth is not only controlling of growth direction and diameter of nanowires but also avoidance of tapering during growth. This would allow realizing longitudinal heterostructures without any undesired growth along the radial direction.

Figure 4a shows a high-resolution TEM image of the interface between the Si and the Ge region. The upper part with dark contrast is Ge and the lower part is Si, respectively. The interface of every nanowire showed a concave shape, which was not reported for SiGe−Si heterostructures.[8,9] The strong dark contrast at the left edge of the interface is an Au particle remaining after wire growth. Figure 4b shows an image obtained by Fourier transformation filtering of an enlarged view of the area indicated as a box in Figure 4a. The Si part in the nanowire was homoepitaxially grown on the Si(100) substrate, and its growth direction was [100]. Moreover, we could observe that Ge[100] is parallel to Si[100], and the Ge part of the nanowire was grown epitaxially on the Si[100] nanowire. The lattice constant of the Ge nanowire estimated from the image and using the image of the Si substrate as a reference was 0.56 nm. This is in good agreement with the bulk Ge lattice constant of 0.567 nm.[16] The dislocations are indicated as "T" symbols in Figure 4b. We observed two different types of dislocations at the interface, which were the expected dislocations relaxing the lattice misfit and dislocation loops. Therefore, the overall observed dislocations showed a complicated pattern and were difficult to distinguish from each other. We think that the dislocation loops were introduced by an imperfect surface of Si due to remaining Au. Distortion contrast can be seen around such dislocations in Figure 4b as dark contrast. The origin of the convex interface might be understood as a result of the special temperature sequence used during growth. The Si dissolved in the Si−Au eutectic is precipitated during cooling below the eutectic temperature. If ⟨111⟩ Si surfaces grow preferentially, the result might be a truncated pyramid of Si with {111} side surfaces and a flat (100) top surface.

The Au metal sits on top of the pyramid. After the Ge precursor is introduced, the temperature rises again and Ge starts to grow on top of the truncated Si pyramid. The phase digram of Ge−Au allows the VLS growth mode and at temperatures below the eutectic temperature Ge can be dissolved in a smaller concentration in solid Au. This leads to the VSS (vapor−solid−solid) growth mode of Ge on Si, which allows a relatively sharp interface between Si and Ge. This is in contrast to experiments using VLS growth only, where the Si dissolved in the liquid is replaced continuously by Ge and the interface is smeared out.

Au-catalyzed vertical Ge nanowires were grown on a bare Si(100) substrate and in an AAO membrane using lowly toxic *n*-butylgermane as precursor. Ge nanowires could be grown in the temperature range from ∼370 to 470 °C. On the bare Si(100) substrate, the Ge nanowires were grown along Si ⟨111⟩ and ⟨110⟩ directions. In the AAO pores, the growth direction of the wires was forced perpendicular to the substrate along the Si[100] direction, and epitaxial Ge/Si heterostructure nanowires were prepared. The interface between Ge and Si has a distinct convex shape which was not reported in previous studies of Ge/Si nanowire growth. The relatively sharp interface between Si and Ge might be the result of VSS growth of Ge.

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