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Extended Arrays of Vertically Aligned Sub-10 nm Diameter [100] Si Nanowires by Metal-Assisted Chemical Etching

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ABSTRACT

Large-area high density silicon nanowire (SiNW) arrays were fabricated by metal-assisted chemical etching of silicon, utilizing anodic aluminum oxide (AAO) as a patterning mask of a thin metallic film on a Si (100) substrate. Both the diameter of the pores in the AAO mask and the thickness of the metal film affected the diameter of SiNWs. The diameter of the SiNWs decreased with an increase of thickness of the metal film. Large-area SiNWs with average diameters of 20 nm down to 8 nm and wire densities as high as 10^{10} wires/cm^2 were accomplished. These SiNWs were single crystalline and vertically aligned to the (100) substrate. It was revealed by transmission electron microscopy that the SiNWs were of high crystalline quality and showed a smooth surface.

In recent years silicon nanowires (SiNWs) have attracted much attention[1,2] due to their many unique properties and potential applications as building blocks for advanced electronic devices,[3,4] biological sensors,[5,6] and optoelectronic devices,[7,8] as well as for renewable energy devices.[9] As in many applications of nanostructured materials, it is important not only to synthesize SiNWs with a high degree of regularity and uniformity in terms of diameter and length, but also to accurately position them in arrays. Fabrication of spatially well-resolved two-dimensional (2D) periodic arrays of vertically aligned epitaxial SiNWs with controlled density is of utmost importance for many practical applications, such as in field-effect transistors (FET).[3,4] To date, considerable efforts have been devoted to fabricating vertically aligned SiNWs.

As a bottom-up approach, the vapor−liquid−solid (VLS) growth method[10] utilizing catalytic metal nanoparticles is known to be a general way of the epitaxial growth of SiNWs with some degree of controllability over diameter and wire density.[11,12] However, tight control over the diameter and spacing of SiNWs is rather difficult to achieve unless colloidal catalytic metal particles with a tight diameter distribution or electron beam lithography are used. Moreover, easy application of the technique is limited to a specific crystallographic orientation (i.e., ⟨111⟩). Vertical epitaxial growth of SiNWs on Si (100) wafers, which are conventionally used in current CMOS technology, still remains a challenge due to the preferred growth directions of SiNWs to ⟨111⟩, ⟨112⟩, and ⟨110⟩ depending on the diameter.[13] Guided epitaxial growth of [100] SiNWs on Si (100) has been recently demonstrated by utilizing anodic aluminum oxide (AAO) as a template.[14,15] However, the approach requires a preannealing of AAO above 800 °C prior to seeding of catalytic gold nanoparticles and an ultrahigh vacuum (UHV) system for subsequent VLS growth of nanowires. In addition, this approach has presently not yet been shown to work for nanowire diameters below about 60 nm.

As a top-down approach, metal-assisted wet-chemical etching of silicon substrates[16−19] in combination with nanosphere lithography[20] is considered as a promising solution to achieve precise positioning of aligned SiNWs as well as control of diameter, length, spacing, and density, avoiding high-cost and low-throughput conventional lithographic processes.[21,22] In this method, a hexagonal array of nanospheres on a silicon substrate acts as a patterning mask for a thin metallic film with an array of holes. The Si surface that comes in contact with the metal is selectively etched, leaving behind arrays of SiNWs whose diameter is predefined by the size of holes in the metal film, while the length is determined by the etching time. Vertically aligned arrays of SiNWs of relatively large diameters (100 nm and larger) were

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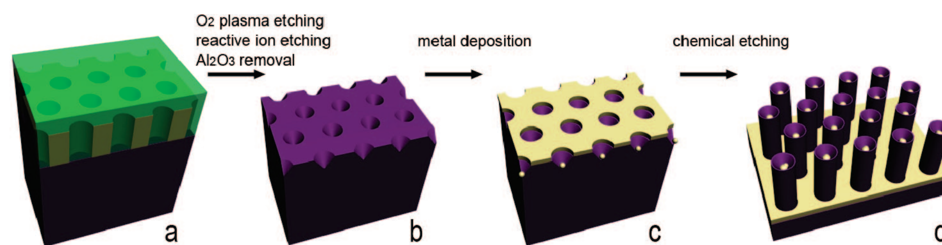

Figure 1. Schematics of the fabrication process.

recently demonstrated on (100)- or (111)-oriented silicon substrates.[21,22] However, the nanosphere approach is difficult to realize for SiNWs with diameters smaller than 20 nm. Apart from achieving 2D extended ordered arrays of spatially well-separated sphere masks, it is hard to ensure successful patterning of a metal film with arrays of discrete holes, when the size of the spheres is reduced down to 20 nm and below, and thus comparable to the typical thickness of the metal film to be deposited.

Here, we demonstrate that metal-assisted etching combined with surface prepatterning of silicon substrates can successfully be used for the fabrication of spatially well-separated 2D periodic arrays of vertically aligned [100] SiNWs with diameters as small as 8 nm on Si (100) substrates. In the present study, ultrathin AAO membranes with regular hexagonal ordered arrays of pores were used as masks for the surface prepatterning of silicon substrates prior to metal-assisted etching of silicon and allowed us to circumvent the problems associated with the conventional nanosphere-based lithographic approach. Ultrathin AAO membranes have been utilized as versatile masks for fabricating 2D extended arrays of various functional nanostructures[23−25] because of the unique ability to control the pore size and pore density (i.e., interpore distance) by varying the electrochemical parameters (e.g., voltage and electrolyte) used in the anodization reaction of aluminum. AAO membranes with pore sizes ranging from 20 to 350 nm and pore densities from $5 \times 10^8/cm^2$ to $3 \times 10^{10}/cm^2$ can conveniently be prepared by anodization of aluminum.[26,27]

The basic experimental procedure employed in the present work is schematically illustrated in Figure 1. First, an ultrathin AAO membrane/polystyrene (PS) composite (thickness = ca. 300 nm) was placed on a (100)-oriented silicon substrate (n-type, resistivity, ρ: 6∼10 Ωcm) that was precleaned by a standard RCA procedure[24,28] (Figure 1a, Supporting Information). PS that was spin-coated to stabilize ultrathin AAO membrane was removed by oxygen plasma (40 sccm, 10 mTorr, 150 W, 5 min). Subsequently, reactive ion etching (RIE) was performed to pattern the surface of Si (100) substrate under SF_6/O_2 plasma (40 sccm, 10 mTorr, 200 W, 30s) in a Plasmalab System100 (Oxford Instruments, U.K.), followed by removal of the ultrathin AAO mask by using RCA solution (80 °C; Figure 1b). Scanning electron microscopy (SEM) investigations on the resulting sample revealed that the hexagonal pattern of the AAO mask was successfully transferred onto the underlying Si substrate with a high degree of fidelity. Subsequently, a thin layer of silver or gold was deposited onto the patterned Si (100) substrate in a sputter coater (208HR, Cressington, U.K.), equipped with a high resolution thickness monitor (MTM-20, Cressington, U.K.; Figure 1c). The diameter of the pores in the metal film caused by the etchpits decreased as a function of deposition time. In other words, there was a closure effect of the pores of the metal film which led to progressive shrinkage of the aperture size as the deposition proceeded.[23] Because of this closure effect, the sputtering process resulted in a uniform coating of metal both on the top surface and on the pore bottom of the patterned Si (100) substrate, but not on the side walls of the pores, as schematically illustrated in Figure 1c and shown in Figure 2b. Finally, ordered arrays of vertically aligned SiNWs on Si (100) substrate were obtained by performing metal-assisted etching of silicon in a mixture solution of hydrofluoric acid and hydrogen peroxide ($HF/H_2O_2/H_2O$, v/v/v = 10/5/35) at room temperature (Figure 1d). The etching was conducted for 10 to 30 s in a dark condition, followed by rinsing of the resulting sample in deionized water.

Figure 2a shows a representative cross-sectional SEM micrograph of a sample after RIE treatment. The ultrathin AAO mask was partly removed in order to visualize both the mask and the arrays of holes on the patterned Si substrate. In this specific case, pore diameter, interpore distance, and pore density of the AAO mask used in the experiment were estimated to be 20 nm, 60 nm, and $2.9 \times 10^{10}/cm^2$, respectively. An oblique angle SEM image of the Si substrate after silver deposition is shown in Figure 2b. Silver at the bottom of each hole exists as a discrete particle disconnected from the silver film on the surface of the silicon substrate. It had been expected that both the silver film on the surface of silicon substrate and the silver particles at the bottom of the holes would participate in the chemical etching of the underlying silicon. Interestingly, however, it turned out that the rate of chemical etching by the silver film was much faster than that of silver particles, resulting in arrays of axially aligned SiNWs on a silicon substrate, as evidenced by the SEM micrograph shown in Figure 2c where a silver particle on top of each SiNW can clearly be seen.

The origin of the strongly different silicon etching rates induced by the metal film and the metal particle is not understood at the moment. Different accessibility of etching solution to Si might be responsible for the different etching rate, as reported recently.[29] However, this diffusion controlled etching can not reasonably account for the slower rate of etching at the interface of the metal nanoparticles and Si, where mass transport is believed to be much easier than that at the interface of the metal film and Si because of geometric

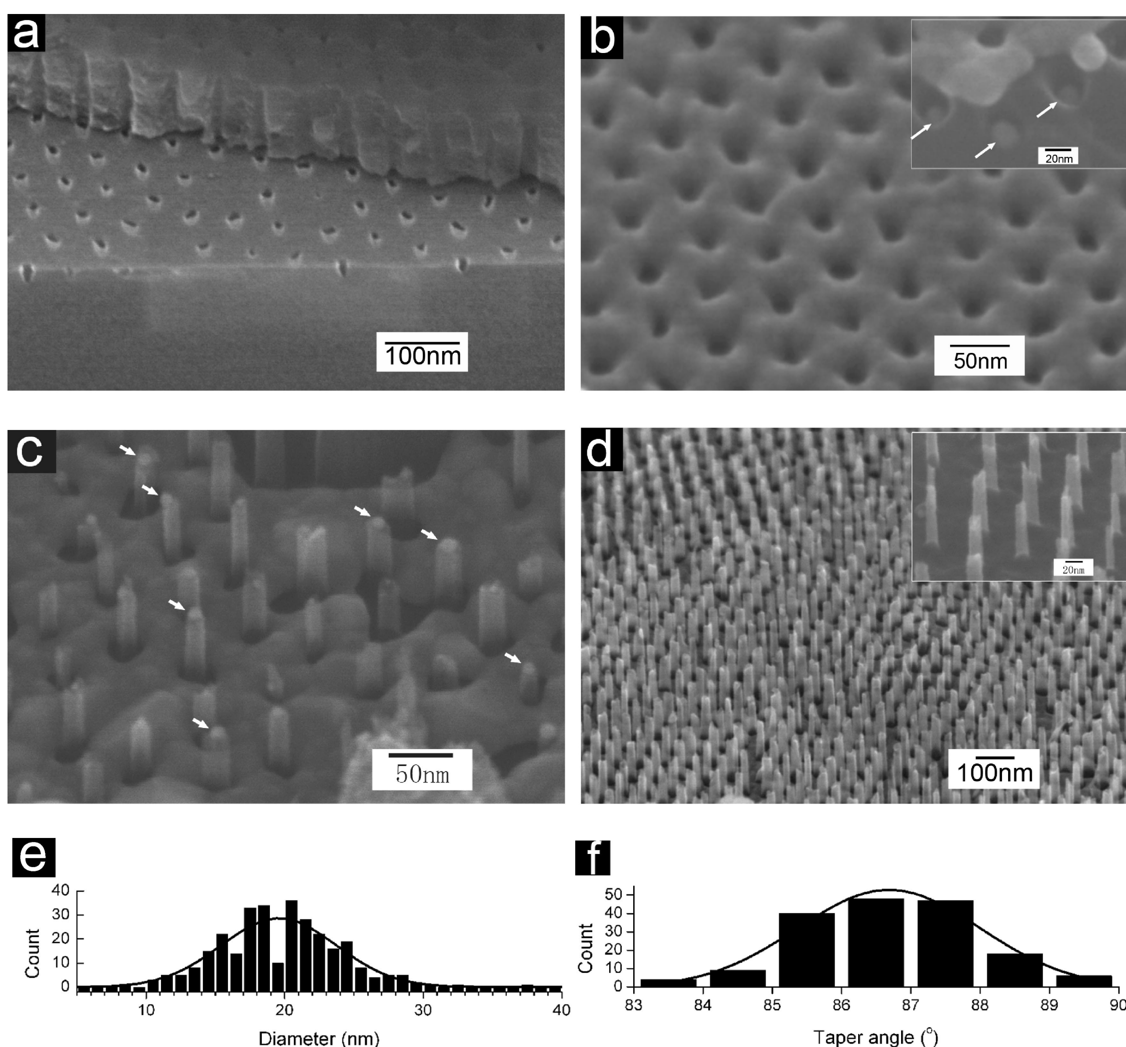

Figure 2. (a) SEM image of AAO mask and pores on a Si (100) substrate. (b) SEM image of the patterned Si substrate after the metal deposition. The inset shows an SEM image of a cross-sectional sample, on which the metal particles are marked by arrows. (c) SEM image of the Si substrate after chemical etching, from which the metal film was not removed. Some large metal particles are marked by arrows. (d) SEM image of SiNW arrays fabricated by chemical etching. The inset shows a large magnification SEM image of SiNW arrays. The statistical distribution for (e) the diameter and (f) the taper angle of SiNWs. The bar represents the measured statistical data and the line is a Gaussian fitting. For SEM images presented in this figure, all samples were tilted by 45 ° during the observation.

reason. Another possible reason might be the different barrier height of the Si/film contact and the Si/particle contact. It has been shown by simulation[30] and experiment[31] that the Schottky barrier height of semiconductor/metal contact increases when the size of metal feature decreases. In the present study, the diameter of the metal particles at the bottom of the pore is less than 20 nm, while the width of the metal film between two pores is larger than 40 nm. Hereby, it is expected that the Si/film contact has a barrier height smaller than the Si/particle contact. Accordingly, it is easier for electrons to transport through the Si/film contact than through the Si/particle contact. Therefore, the etching assisted by the metal film might be faster than that by metal particles. Alternatively, it might also be speculated that the surface of the etchpits were modified by the reactive ion etching process in such a way that metal-induced etching is not possible any more. Clearly, a more systematic study is needed to unravel the reason for the observed etching efficiency, which is critical for the success of our process.

Figure 2d shows extended arrays of vertically aligned SiNWs after removal of silver by using HNO_3. Upon close examination, it is clear that the SiNWs have smooth surfaces. On the other hand, the shape of the SiNWs is characterized by a tapered morphology with different diameters at the top and the bottom part (see the inset of Figure 2d). The evolution of the tapered morphology might be attributed to the dissolution of metal during the etching. Silver, which was the metal used to assist the etching of Si in the present experiments, could be partially dissolved by the etching solution.[29,32] During the etching, the silver was gradually dissolved, and the diameter of the holes on silver film could gradually increase. Accordingly, the diameter of SiNWs would become larger with the evolution of etching. Alternatively, a slight isotropic etching of silicon in $HF-H_2O_2$ solution will cause a smaller diameter of the nanowire parts exposed for a longer time to the etching solution which also leads to tapering.

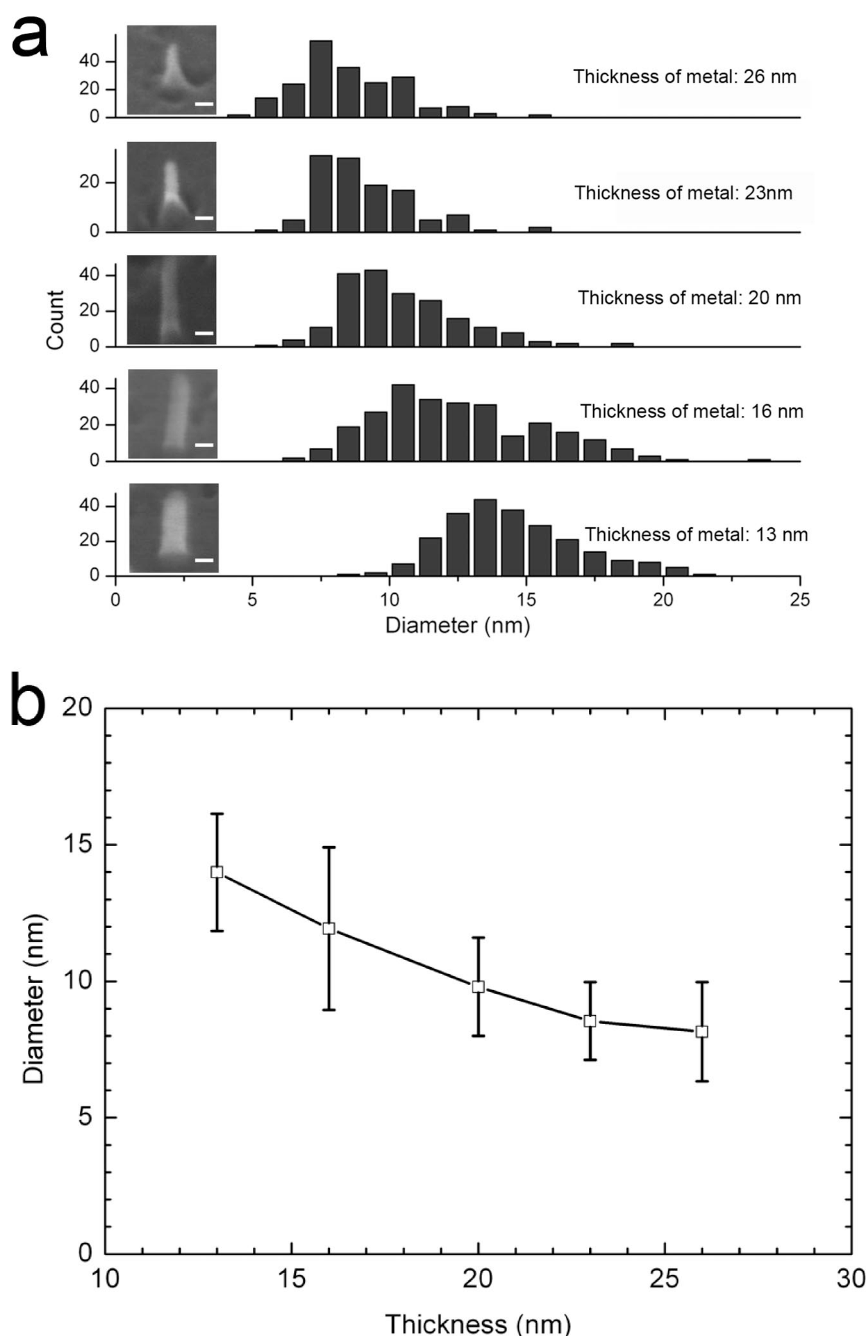

Figure 3. (a) Diameter distribution of SiNW arrays fabricated with the metal films of different thicknesses. The insets show typical SEM images of SiNWs fabricated with the metal films of different thickness. (scale bars = 10 nm). (b) Relationship of the thickness of the metal film and the average diameter of SiNWs.

In order to get quantitative information on the size distribution of the present SiNWs, image analyses were carried out on the basis of SEM micrographs. The average diameter was measured at the middle part of SiNWs, while the average tapered angle was measured from the angle between sidewall and axis of the SiNWs. According to statistical analysis, in this specific case, the average diameter and tapered angle of SiNWs were measured to be 19.6 ± 4.2 nm and 86.7 ± 1.3°, respectively.

As discussed earlier, the aperture of the metal film decreases with deposition time because of the closure effect (vide supra). It implies in turn that the diameter of the remaining pores in the metal film decreases with the thickness of the deposited metal film. Accordingly, it is possible to control the diameter of SiNWs by varying the thickness of the metal film, since the diameter of SiNWs in the present process is determined by the diameter of the remaining pores in the metal film. Figure 3 show the evolution of wire diameters as a function of the thickness of metal film. It is clear from the figure that the average diameter of SiNWs is approximately inversely proportional to the thickness of the metal film. An average diameter of the SiNWs as small as about 8 nm could be realized (Figure 3). All SiNWs shown in the insets of Figure 3a have an aspect ratio larger than 4, which is large enough for the fabrication of excellent wrap-around transistors.[33] The aspect ratio can be further increased

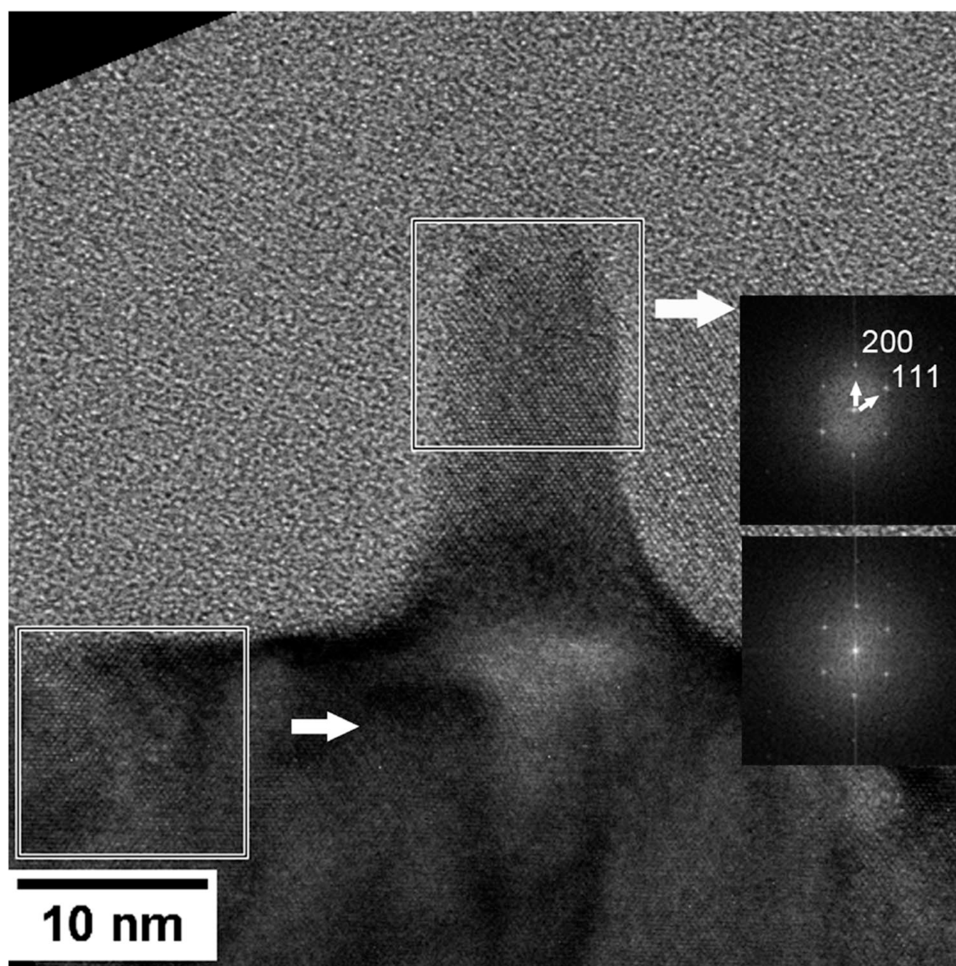

Figure 4. HRTEM cross-sectional image of a 10 nm SiNW fabricated by using etching assisted by a 20 nm thick gold film. The squares outline the regions used for FFT. The upper FFT pattern corresponds to a region in the SiNW, and the lower one corresponds to a region within the silicon (100) substrate.

by simply increasing the etching duration,[21] if a larger aspect ratio would be required.

We found that the number of sites where SiNWs are missing increases with the thickness of the metal film (see Supporting Information). This phenomenon can be understood by considering the variation of the original pore diameter on the patterned Si substrate and the closure effect during the metal deposition. Because of the variation of the pore diameter on the patterned Si substrate, there are some pores which have diameters small enough to be sealed by the metal deposition according to the closure effect. These closed pores obviously could not evolve into SiNWs after etching. When the thickness of the metal film is increased, more and more pores are sealed because of the closure effect, and accordingly, the number of sites where SiNWs are missing increases.

In order to get insight into the crystallinity of SiNWs, a high resolution transmission electron microscopy (HRTEM) investigation was carried out. Figure 4 shows a representative HRTEM image of a single SiNW fabricated with a 20 nm thick metal film, revealing clearly that SiNWs prepared by the present method are highly crystalline with very smooth surface without defects. In the literature, it has been reported that, in metal-assisted etching, the freshly prepared surface was smooth[21] and the surface became rougher with etching time because of the random etching of Si by the etching solution.[21,34] Since the rate of the random etching was much slower than that of etching assisted by the metal film, the etching time was short enough (30 s) in our experiments to avoid the random etching, and accordingly, the SiNWs had a smooth surface.

The axial orientation of SiNW was investigated by fast Fourier transform (FFT) of the HRTEM images. As shown in Figure 4, the FFT pattern from the SiNW is identical to that from the Si (100) substrate, and the axial orientation of SiNW is along the [100] direction. The results presented in Figure 4 suggest that we can obtain vertically oriented SiNWs with high crystalline quality on Si (100) substrates.

In summary, metal-assisted etching combined with surface prepatterning of silicon substrates was successfully employed to fabricate spatially well-separated 2D ordered arrays of vertically aligned SiNWs on (100) silicon wafers. The average diameter of SiNWs was observed to decrease with increasing thickness of the metal film used to assist the etching. SiNW arrays with average diameters as small as about 8 nm and with a density of wires as high as 10^{10} wires/cm^2 were fabricated. The SiNWs showed a high crystalline quality and a smooth surface.

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Supporting Information Available: Experimental details on the fabrication of anodic aluminum oxide. SEM micrograph of SiNW fabricated with metal films of different thicknesses. This material is available free of charge via the Internet at http://pubs.acs.org.

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