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Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor

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Semiconducting nanowires have recently attracted considerable attention. With their unique electrical and optical properties, they offer interesting perspectives for basic research^[1] as well as for technology. A variety of technical applications, such as nanowires as parts of sensors,^[2] and electronic^[3,4] and photonic devices^[5] have already been demonstrated. In particular, electronic applications come more and more into focus, as the ongoing miniaturization in microelectronics demands new innovative solutions. Semiconducting nanowires, in particular epitaxially grown silicon (Si) nanowires, are considered as promising candidates for post-CMOS (CMOS: complementary metal–oxide semiconductor) logic elements owing to their potential compatibility with existing CMOS technology. One major advantage of vapor–liquid–solid- (VLS-) grown nanowires compared to top-down fabricated devices is that they have well-defined surfaces. This reduces surface scattering, an issue which becomes important for devices on the nanoscale. Moreover, epitaxially grown nanowires circumvent the problem of handling and positioning nanometer-sized objects that arises in the conventional pick-and-place approach, where devices are fabricated by manipulating horizontally lying VLS-grown nanowires.^[6] The first step towards a technical realization of a nanowire logic element is the design and manufacturing of a nanowire transistor. The epitaxial growth of vertical nanowires offers advantages over other approaches: For example, the transistor gate can be wrapped around the vertically oriented nanowire. Such a wrapped-around gate allows better electrostatic gate control of the conducting channel and offers the potential to drive more current per device area than is possible in a conventional planar architecture.^[7]

In this Communication, a generic process for fabricating a vertical surround-gate field-effect transistor (VS-FET) based on epitaxially grown nanowires is described. Exemplarily, we used Si nanowires and present a first electrical

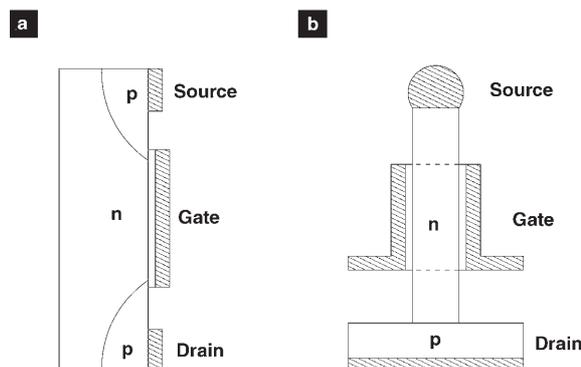


Figure 1. Schematics of a) a conventional p-channel MOSFET and b) a silicon nanowire vertical surround-gate field-effect transistor.

characterization proving the feasibility of the process developed and the basic functionality of this device.

Figure 1a shows a schematic cross section through a conventional p-type MOSFET. In such a device, an inversion channel can be created close to the gate by applying a negative gate voltage. This forms a conducting channel that connects the p-doped regions between the source and drain contacts electrically. Using this concept, a silicon nanowire VS-FET would ideally require a nanowire that is n-doped in the region of the gate and p-doped elsewhere. Unfortunately, such a p-n-p structure with abrupt transitions appears difficult to realize if the nanowires are grown by means of the vapor–liquid–solid mechanism^[8] using gold as a catalyst. The difficulty here is that the dopant atoms, which are dissolved in the catalyst droplet, might act as a reservoir, thus creating a graded transition when switching to another dopant.

Therefore, we used a structure consisting of an n-doped silicon nanowire grown on a p-type substrate (see Figure 1b). If the gate–drain and gate–source distances are not too long, it is electrostatically still possible to create an inversion channel along the length of the entire wire. In the proposed configuration, the p–n junction at the source contact (Figure 1a) is replaced by a Au/n-Si Schottky contact at the nanowire tip.

In order to investigate the influence of the Au/n-Si Schottky contact on the nanowire (current–voltage) I – V characteristics, an array of n-doped nanowires vertically grown on an n-type (111)-oriented substrate was imbedded in a spin-coated SiO₂ matrix. After removing the thin SiO₂ coverage from the Au tips by a short reactive ion etching, contacts 0.6 mm² in size were defined by evaporating aluminum onto the sample, such that approximately 10⁶ nanowires were contacted in parallel. The temperature-dependent measurements (shown in Figure 2) were performed by applying a voltage to the Si substrate, while the Al top contact was held at a constant potential. The measurements reveal a strong rectifying behavior with a thermally activated current possessing an activation energy of 0.6 eV. This can be explained by the Au/n-Si Schottky contact dominating the I – V behavior. The fact that the Schottky contact is forward-biased for negative voltages furthermore proves that, as expected, electrons act as majority charge carriers.

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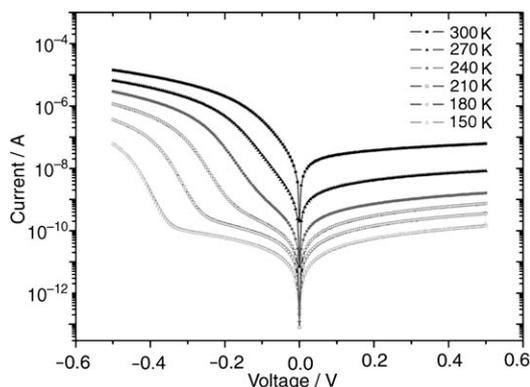


Figure 2. Temperature-dependent current–voltage characteristics of an array of n-doped silicon nanowires.

The Si nanowires used were epitaxially grown by chemical vapor deposition (CVD) on a (111)-oriented p-type Si substrate. A detailed description of the growth process is given in the Experimental Section and in Ref. [9]. The nanowire growth parameters were chosen so that the majority of the nanowires were [111] oriented, that is, that the nanowires grow perpendicular to the substrate, as schematically shown in Figure 3a. The typical average diameter of

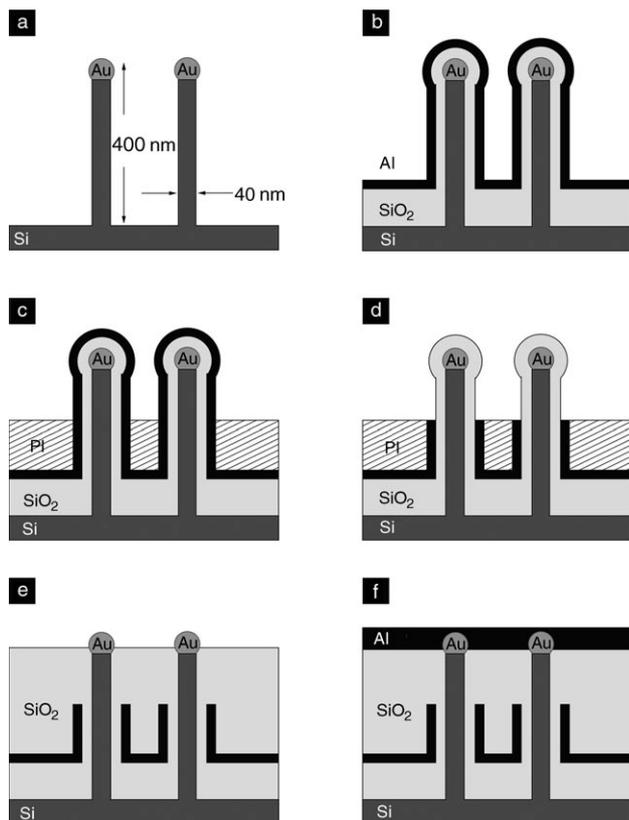


Figure 3. Nanowire VS-FET process flow. a) Vertically grown silicon nanowires. b) After deposition of SiO₂ layers and Al gate metal. c) After polyimide (PI) deposition and polyimide RIE etching. d) After Al wet-chemical etching, and SiO₂ RIE etching. e) After polyimide removal, SiO₂ deposition, and SiO₂ RIE etching. f) After deposition of Al as source metal.

the nanowires was 40 ± 5 nm. The p-type Si substrate was metallized to create a backside electrical contact as the drain contact.

The first step of the VS-FET processing was the deposition of the SiO₂ gate insulator. The Si nanowires were encapsulated with a uniform, approximately 10-nm-thick SiO₂ layer grown by CVD as gate dielectric. In the second step, a spin-on-glass (Futurrex IC1-200) is deposited by spin-coating and then thermally cured at 400 °C for 30 min under nitrogen. This additional SiO₂ layer electrically isolates the metal gate from the Si substrate and thus the drain contact so that leakage currents are avoided. As gate metal, an aluminum layer is deposited by e-beam evaporation to cover the SiO₂-encapsulated Si nanowire with an uniform thickness of 30 nm. A schematic of the sample after these processing steps is shown in Figure 3b.

Afterwards the sample was spin-coated with a layer of polyimide (HD Microsystems), which was thermally cured at 350 °C for 30 min. The polyimide layer serves as an etch-stop for the subsequent wet-chemical etching step that removes the upper part of the gate metallization (see Figure 3d). To define the gate length, the polyimide was etched down in a reactive ion etching (RIE) system (Oxford Plasmalab) until the nanowire tips extended about 150 nm above the polyimide surface (see Figure 3c). Then, the sacrificial polyimide layer was entirely removed by an O₂ plasma treatment.

In the next step, the Si nanowires were completely embedded in SiO₂ by spin-coating a sufficiently thick layer of spin-on-glass on top of the sample followed by thermal curing. RIE is used to free the Au/Si caps of the nanowire tips from the SiO₂ deposited (see Figure 3e). Finally, a 100-nm-thick layer of Al or Ti was deposited to contact the Au-covered nanowire tips and thus establish the source contact. An advantage of this process is that the fabrication of the VS-FET does not include any chemical/mechanical polishing step. In addition, the process flow developed is generic and can therefore be used with any other nanowire/substrate combination.

A transmission electron micrograph (TEM; Philips CM20) of the resulting VS-FET is shown in Figure 4. Because of the low contrast of Al compared with Si or SiO₂, this TEM-image is reproduced in Figure 4b with the Al and

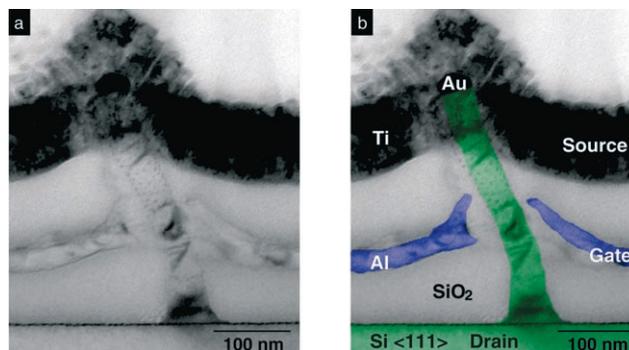


Figure 4. a) TEM of a silicon nanowire VS-FET (exclusively produced for TEM study). b) Colored TEM image (green: silicon, blue: aluminum).

Si colored in blue and green, respectively. One can clearly see the nanowire, epitaxially grown on the Si surface, with the gate surrounding the nanowire approximately midway along its length. The bending of the nanowire is probably due to stress during the spin-on-glass coating step and/or the polyimide curing.

For the electrical measurements, the nanowires were grown on the substrate in stripe-shaped regions of a few hundred micrometers in width. The gate and source contacts were defined using optical lithography and lift-off techniques. Figure 5a shows a top-view optical micrograph of

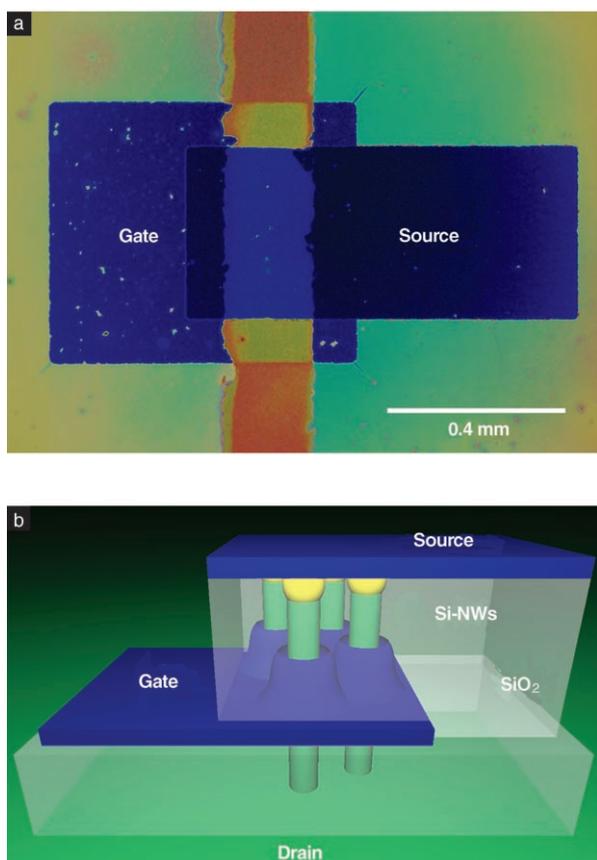


Figure 5. a) False-colored top-view optical micrograph of the contact arrangement. The red and yellow stripe is the region where nanowires are grown. The gray-green areas to the left and right are regions without nanowires. The blue areas are the Al source and gate contact. b) Schematic 3D side-view of the contact arrangement.

the contacts. The active area where nanowires are contacted is on the order of 10^{-1} mm^2 and is defined by the width of the source contact and the width of the stripe. The average distance between individual nanowires is about $1 \mu\text{m}$, which translates to an estimated 10^4 to 10^5 silicon nanowires contacted in parallel by the source and drain contact. A schematic 3D picture (Figure 5b) illustrates the vertical position of the different layers. To contact the gate electrically, it was necessary to remove the SiO_2 layer that covers the gate contact. This was achieved in an anisotropic RIE step, using the metal source contact as an etching mask.

Electrical measurements were performed using an Agilent 4155C parameter analyzer. The output characteristics of a Si nanowire VS-FET device (10^4 to 10^5 silicon nanowires contacted in parallel), processed with the method described are shown in Figure 6a for gate voltages V_G be-

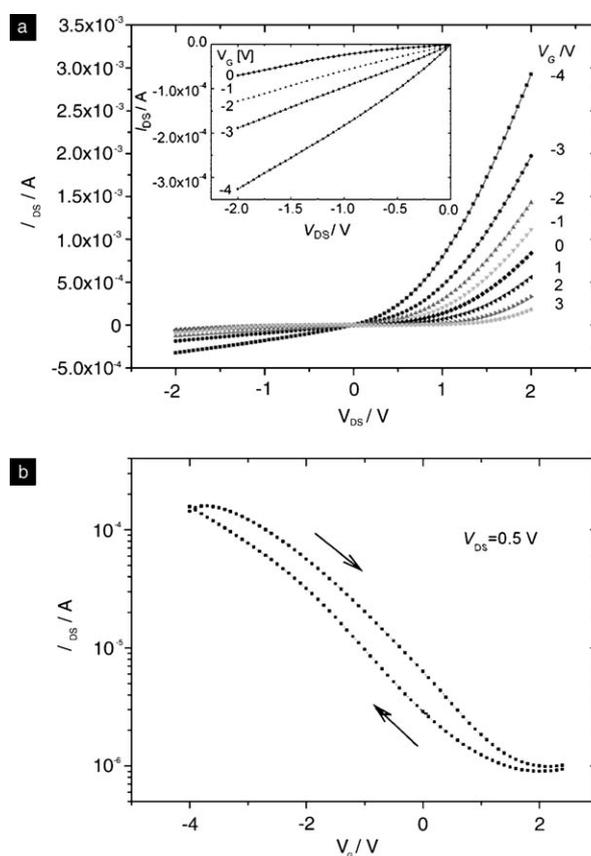


Figure 6. a) Output characteristics of an array of VS-FETs for different gate voltages. b) Drain–source current I_{DS} versus gate voltage V_G , $V_{DS} = -0.5 \text{ V}$.

tween $+3$ and -4 V . For positive drain–source voltages V_{DS} , the drain–source current I_{DS} strongly depends on V_G . With increasing negative V_G values, the drain–source current increases, whereas with increasing positive V_G it is reduced. For negative V_{DS} values, the gate-voltage dependence of I_{DS} is similar but less pronounced. Such a behavior is characteristic of hole transport and is indicative of the gate-driven formation of an inversion layer of holes in the vicinity of the gate. In the case of inversion, the holes in the inversion channel can inundate the n-doped nanowire. Thus, for negative V_G , our Si nanowire VS-FET seems to function as a normal p-channel MOSFET. The nanowire VS-FET is normally on, and turns off only if a positive gate voltage is applied. This indicates a shift of the threshold voltage that can be attributed to trapped and/or interfacial charges.

Considering the characteristic of a p-channel MOSFET, one would expect a linear behavior of I_{DS} at low V_{DS} values in the third quadrant, followed by a saturation of I_{DS} as V_{DS} increases. The inset of Figure 6a shows a close up of the third quadrant: For small values of V_G , the increase of I_{DS} at

low V_{DS} values is nonlinear, indicating a series resistance that might be attributed to an incomplete formation of the inversion channel close to the interface of the p-type substrate and the n-type nanowires. Therefore, no extraction of a charge-carrier mobility in the linear regime can be performed. Moreover, for the VS-FET no saturation of I_{DS} can be observed, as is the case for other nanowire FETs.^[4,10] In addition, the inset of Figure 6a shows that the on/off ratio at $V_{DS} = -0.5$ V is approximately 6.

In Figure 6b the drain-source current I_{DS} at $V_{DS} = 0.5$ V is plotted versus V_G . Considering the number of nanowires contacted in parallel, it is most remarkable that the current changes by more than two orders of magnitude if the gate voltage is decreased from +2 to -4 V. As discussed above, this effect can be explained by the creation of an inversion channel in the nanowire. The small slope of the curve in Figure 6b might be due to interface charges located at the Si/SiO₂ interface. The existence of charged traps at the Si/SiO₂ interface could possibly also explain the hysteresis observed in Figure 6b.

In conclusion, we have presented a generic process flow to fabricate silicon nanowire vertical surround-gate field-effect transistors (VS-FET). The intrinsic advantage of the process developed is that no chemical or mechanical polishing steps, which are difficult to control at this length scale, are needed. In the demonstrated device, n-doped silicon nanowires grown epitaxially on a p-doped substrate were used as active material. The array of VS-FETs exhibited a gate-voltage-dependent current increase of more than two orders of magnitude.

Experimental Section

The silicon nanowires were produced by chemical vapor deposition (CVD) in an ultrahigh vacuum (UHV) environment. For this purpose, (111)-oriented boron-doped ($> 5 \Omega\text{cm}$) 100 mm silicon wafers were cleaned (RCA cleaning), dipped into diluted hydrofluoric acid, and immediately transferred into the UHV system. A few angstroms of gold were deposited in situ onto the hydrogen-terminated silicon in stripes of a few hundred micrometers in width by means of a shadow mask. A radiative heater was used to anneal the wafer at 450 °C for 30 min to break up the gold film and create the Au/Si eutectic droplets necessary for nano-

wire growth. The temperature was then lowered to 320 °C and a small amount of antimony was deposited onto the Au/Si droplets by an e-beam evaporation source in order to inject the dopant into the droplets. The temperature was then raised again to 450 °C, and the UHV-chamber flooded with diluted silane (5% in argon) until a pressure of 1.9 mbar was reached. Under constant pressure, nanowire growth proceeded for a total of 12 min. The resulting nanowires have diameters of around 40 nm and an aspect ratio of ≈ 10 .

Keywords:

chemical vapor deposition • field-effect transistors • nanowires • silicon

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