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Nuclear Instruments and Methods in Physics Research A 511 (2003) 250–256

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

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Design and technology of DEPFET pixel sensors for linear collider applications

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Abstract

The performance requirements of vertex detectors for future linear collider experiments is very challenging especially for the detector's innermost sensor layers. The DEPleted Field Effect Transistor (DEPFET) combining detector and amplifier operation is capable to meet these requirements. A silicon technology is presented which allows production of large sensor arrays consisting of linear DEPFET detector structures. The envisaged pixel array offers a low noise and low power operation. To ensure a high radiation length a thinning technology based on direct wafer bonding is proposed.
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Keywords: Active pixel detector; DEPFET; Low noise operation; Vertex detector; Linear collider

1. Introduction

Active pixel detectors play a growing role in high energy and astrophysics experiments. Future experiments, e.g. TESLA (Tera Electron Volt Energy Superconducting Linear Accelerator) [1] and the XEUS (X-ray Evolving Universe Spectroscopy Mission) [2], will need large area pixel detectors with very challenging requirements. In astrophysics the spatial resolution of the detector is less crucial than the energy resolution, because the degree of spatial precision is limited more by the Wolter X-ray telescopes than by the silicon sensors. The requirements in high energy physics are often opposite.

Especially for the inner layer of the TESLA vertex detector, a lot of partially contradictory demands have to be addressed. In order to meet the required resolution of primary and secondary vertices the very inner detector layer has to be placed at a radius of 15 mm from the interaction point. The pixel detector at this place has to provide a spatial resolution of less than 5 μm. The resulting high occupancy caused by the

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doi:10.1016/S0168-9002(03)01802-3

beamstrahlung has to be suppressed by a very fast readout cycle of about 50 MHz. To reduce multiple scattering the material introduced in the detector has to be kept low. This means that no extra material for cooling pipes, etc. is allowed and additionally the sensor substrates must be thinned to $\sim 50\,\mu m$ thickness. This results in a reduced signal charge compared to that generated in standard silicon detectors, where the depletion layer extensions are of the order of $500\,\mu m$. In summary, the ideal vertex detector for TESLA should fulfill the competing boundary conditions simultaneously: High position resolution should be achieved with small signal amplitudes, i.e. with thin detectors. Simultaneously the operation must be fast, e.g. 20 ns processing time with low power dissipation in an environment of a significant radiation level.

The DEPleted Field Effect Transistor structure, abbreviated DEPFET, is a monolithic device which is integrated onto a high ohmic fully depletable detector substrate [3]. The device is one proposal for a detector design which is consistent to a large extent with all of the above requirements [4]. While the system aspects and the readout concept are discussed in Ref. [5] this paper proposes a technology for the production of large area DEPFET arrays. The different operation modes of the device are evaluated by process and device simulations. A thinning procedure compatible to the DEPFET process and the module concept is discussed.

2. DEPFET operation principles

The DEPFET combines detection and amplification within one device [3]. It is based on the sideward depletion as used in the semiconductor drift chambers [6]. The principle of operation is shown in Fig. 1. A p-channel MOSFET or JFET (junction field effect transistor) is integrated onto a silicon detector substrate, which becomes fully depleted by the application of a sufficiently high negative voltage to a backside p^+ contact. By means of the sideward depletion, a potential minimum is formed which is shifted directly underneath the transistor channel at a depth of

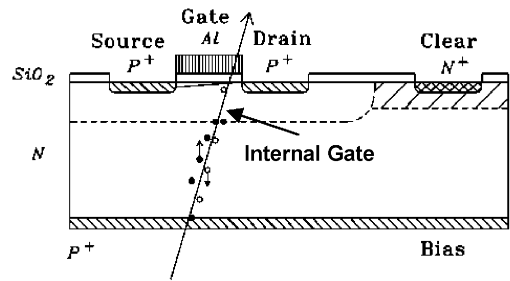

Fig. 1. Cross-section of a DEPFET indicating the operation principle.

about $1\,\mu m$ by an additional phosphorous implantation (see Fig. 1). Incident particles generate electron–hole pairs within the fully depleted bulk. While the holes drift into the back contact, electrons are accumulated in the potential minimum, called the internal gate, resulting in a modulation of the channel current. The readout is non-destructive and can be repeated several times.

The removal of the signal charge and thermally generated electrons from the internal gate is called *Clear*. A neighboring n^+ contact is pulsed at a positive voltage providing a punch-through into the internal gate. This pulsed clear mechanism is discussed below in detail.

Intrinsic advantages of the DEPFET device are the amplification of the signal charge at the position of its generation thus avoiding any charge transfer where losses could occur. The entire bulk is depleted and sensitive to incident radiation. Therefore the non-structured backside can be used as an entrance window thereby improving the spectroscopic performance, especially for low energy photons. The main advantage of the device is its very small input capacitance that provides a very low noise operation even at room temperature. Fig. 2 illustrates the excellent noise performance with a measured ^{55}Fe spectrum.

DEPFET structures can be operated individually, as an integrated on-chip amplifier, for instance in the readout node of a silicon drift chamber, or collectively as a pixel array.

Fig. 3 shows a DEPFET pixel matrix operating with a line-by-line access via the external gates. Note that the external gates just switch the pixel on

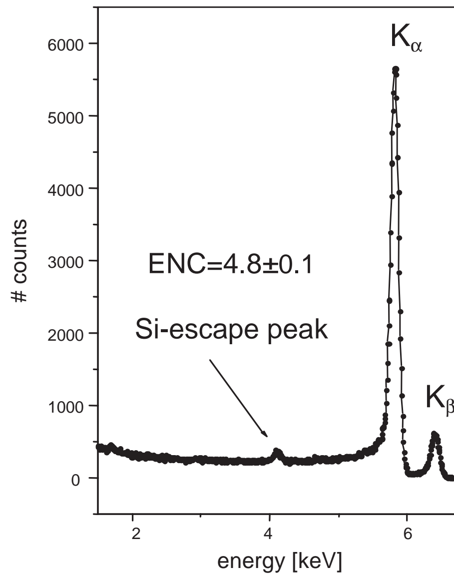

Fig. 2. ^{55}Fe spectrum measured on a single DEPFET pixel at room temperature [8]. The equivalent noise charge was fitted to be ENC = 4.8 ± 0.1.

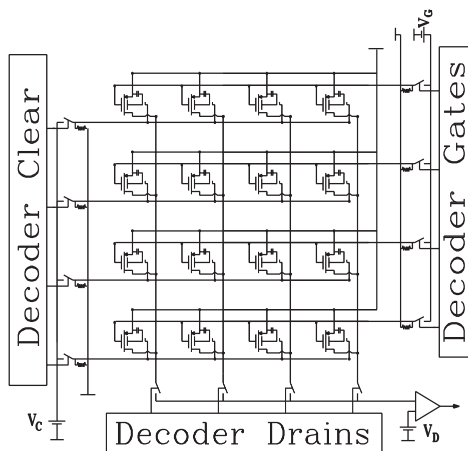

Fig. 3. Basic pixel array readout scheme. Only pixels switched on via the decoder gate. Only the row addressed by the decoder gates is active while the other rows are switched off and do not contribute to power consumption of the detector.

and off while the signal amplification is achieved via the internal gate. There is no current flow in a non-selected DEPFET row, resulting in a very low power consumption of the array [4].

A first 2×2 pixel array was produced and operated in 1997 [7]; results from a 64×64 pixel imaging system were presented in 1999 and 2000 [9–12]. The readout amplifiers at the end of the columns can be connected either to the sources (source follower) or to the drains (drain read out) of the DEPFETs. For linear collider applications we need the faster drain (current) readout (see also Ref. [5]). A measurement cycle consists of a collection stage (*Collect*), the read out (*Read*) and the reset of the internal gate (*Clear*). A pedestal subtraction is obtained by a consecutive *Read–Clear–Read* sequence. Therefore, the clear process affects the noise performance of the device significantly. Any reset noise is avoided if the entire charge is completely removed from the internal gate. If this is not guaranteed an additional noise contribution occurs due to an undefined amount of remaining charge in the internal gate.

3. DEPFET technology development and design

Until now, the DEPFET device concept was evaluated mainly on circularly shaped JFETs.[1] However, a position resolution in the range of $5\,\mu m$ needed for vertexing requires pixel cell sizes of about $25 \times 25\,\mu m^2$. This is impossible to achieve with JFETs at the actually given minimum technological feature sizes of $2 \times 3\,\mu m^2$. Linear structures are innately smaller than circular ones but the fabrication of linear JFETs is very complicated due to the problem of lateral channel isolation. Another intrinsic difficulty of JFET technologies is the pinch off voltage variation over the wafer, within fabrication batches and from batch to batch. Therefore, we are going to use MOS devices. In principle MOSFETs can be produced in any shape, linear as well as circular. In terms of reliability and homogeneity they are suitable for large area devices and have a much higher geometrical scaling potential than JFETs.

For larger area sensor arrays, the availability of more than one metal layer is mandatory due to the necessity of the row- and column-wise connections

[1] 'Circularly shaped' means a closed transistor where the drain surrounds the source region or vice versa, in contrast to linearly shaped transistors having a lateral confinement of the channel by an isolation structure.

of the pixels. At the Semiconductor Laboratory of the Max-Planck-Institutes, a 150 mm silicon technology for MOS type DEPFETs on high ohmic substrates with two polysilicon and two metal layers has been developed. Using the two polysilicon layers, linear DEPMOS transistors can be fabricated whereby the first polysilicon forms a lateral isolation frame and the second one is used for the external gate of the DEPFET. This approach is different from that used in common MOS technologies, where the lateral transistor isolation is provided by locally oxidized field regions or shallow trenches filled with oxide. The channel isolation structure of the DEPFETs must not collect signal electrons and has to accomplish the integration of the clear contacts.

The n^+ doped clear region is close-by the internal gate, separated only by the first polysilicon layer only. In the *Collect* and *Read* modes, the region underneath the polysilicon acts as a potential barrier between the clear region and the internal gate. The barrier has to be overcome during the *Clear* cycle when the clear contact gets positive. The first polysilicon acts not only as an isolation frame but also as a reset (clear) gate. It is held at a constant potential or can be switched in order to alleviate the clear process. As shown in Fig. 4, the linear cell geometry allows for a very compact pixel layout free from potential pockets where the signal charge could disappear (see also Fig. 7). In any case, the implanted drain, source and clear regions are shared by neighboring cells. In this way a small pixel size is achievable even with rather relaxed lithographic requirements. This feature, which defines also the tolerable defect size in the process, is important concerning the yield of large area detectors.

We started a production run on 6 in wafers containing prototype arrays of up to 128×64 pixels for high energy and astrophysical applications [13–15]. The smallest pixel cell size is presently $30 \times 20\,\mu m^2$.

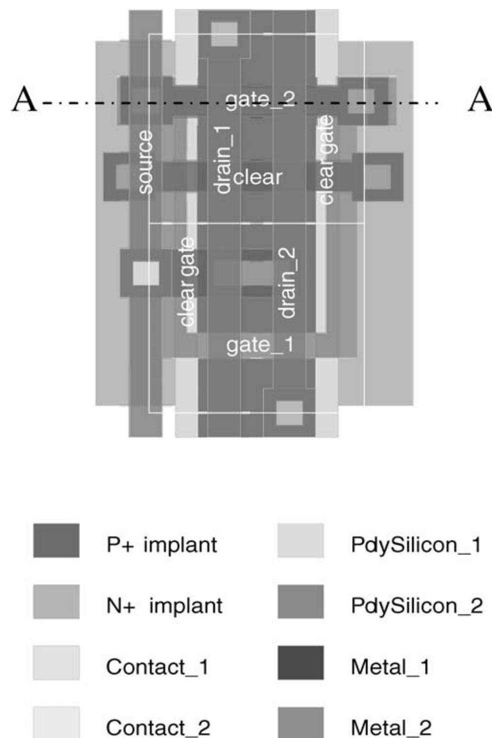

Fig. 4. Layout example for a linear double pixel cell. Each white rectangle surrounds a DEPMOS.

4. Device simulations

Two and three dimensional simulation tools [16–19] are used to optimize the layout and the technology parameters. Fig. 5 shows the simulated potential distribution (Section A-A in Fig. 4) during the clear operation.

The simulation illustrates that the electrons can flow unopposed from the internal gate into the clear contact. The applied clear voltage of 20 V can be reduced by lowering the potential barrier in the clear gate region. During charge collection the transistor is switched off and the potential of the internal gate can be adjusted by the voltage of the external gate via capacitive coupling. Fig. 6 shows the potential at a depth of 1 μm, as seen by drifting electrons generated in the bulk. Note that there is not any attraction of the n^+ clear contact to the electrons at this depth. This is the result of the negative space charge of a deep boron doping implanted beneath the clear region. By switching on the external gate the device current is read out. The drain current response to a given signal charge defines the amplification of the internal gate $g_q = \delta I_D/\delta q$. To analyze the signal response of the

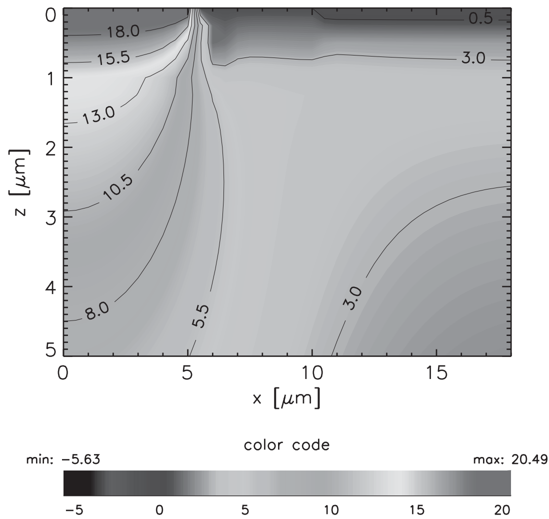

Fig. 5. Potential distribution across the section A-A in Fig. 4 during the clear operation simulated with the 3D-Poisson solver Poseidon [18] ($V_{Clear}=$ 20 V, $V_{Back}=-30$ V, $V_{Source}=0$ V, $V_{Drain}=-5$ V, $V_{Gate}=-3$ V, $V_{Clear\text{-}Gate}=1$ V).

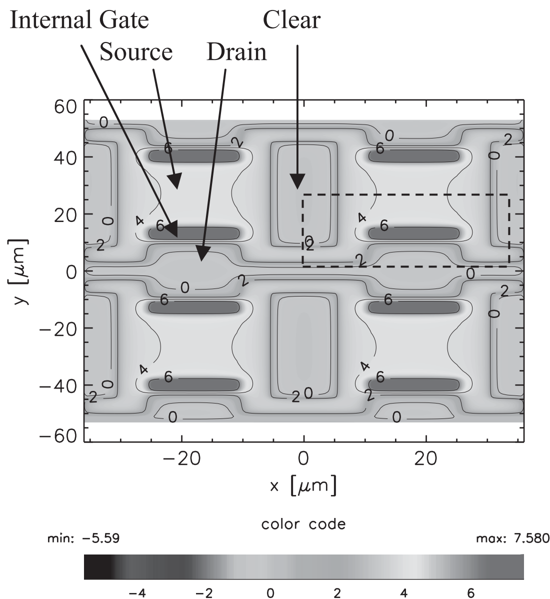

Fig. 6. Potential distribution of a 2 × 4 array section parallel to the surface at a depth of $z=1$ μm during charge collection simulated with Poseidon ($V_{Clear}=3$ V, $V_{Back}=-25$ V, $V_{Source}=0$ V, $V_{Drain}=-5$ V, $V_{Gate}=2$ V, $V_{Clear\text{-}Gate}=1$ V). A single cell is marked by the dashed line.

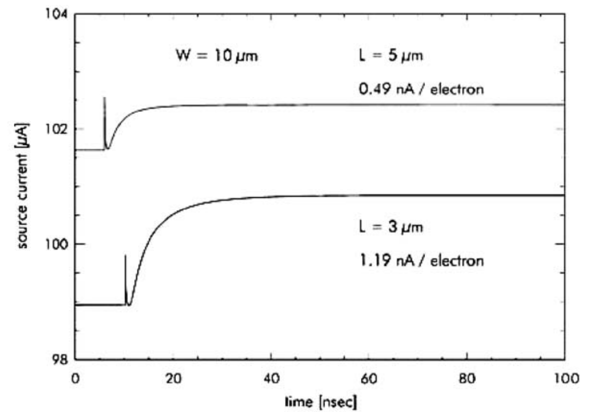

Fig. 7. Simulated signal response to a signal charge generation of 1600 electron–hole pairs

DEPFET, 1600 electron–hole pairs were introduced by a locally and temporally limited increase of the Shockley-Read-Hall generation rate using the two dimensional device simulator TeSCA [16]. The simulated signal response, shown in Fig. 7 demonstrates an amplification potential of more than 1 nA per electron for optimized DEPFET structures.

5. Thinning technology

The DEPFET as a fully depleted device, needs, in addition to the front side structures, a p+n diode at the backside. Therefore a standard thinning process is not applicable because it would destroy the backside pn-junctions. The key technology of the process sequence illustrated in Fig. 8 is the direct wafer bonding [20]. It starts with a sensor wafer on top and a handle wafer on bottom, which are bonded together on their oxidized surfaces (Fig. 8a). The top wafer, which already contains the backside p^+ implantations, is thinned to a thickness of ~50 μm by standard wafer grinding and polishing (Fig. 8b). This side is where the actual device is fabricated. During the front side fabrication process, the obtained sandwich package can be handled like a standard wafer without special precautions for backside protection (Fig. 8c). After topside metallization and passivation. The handle wafer is partially etched

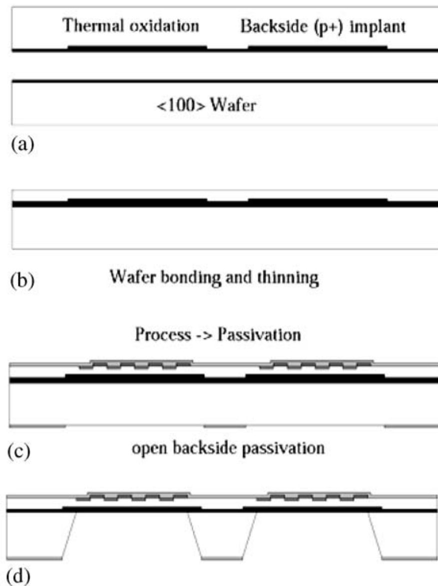

Fig. 8. (a–d) Joint process sequence of wafer thinning and DEPFET production.

back (Fig. 8d) leaving a small frame large enough to provide mechanical stability and space for the affixed steering and readout chips [5].

An inherent advantage of this technology is that the inner silicon oxide acts as a stop layer for the etchant, leaving the backside diode of the sensor wafer unaffected by the etching. With the proposed concept, the material budget per layer can be reduced to the range of 0.1–0.15% of a radiation length including the already thinned read out and line driver chips. Pictures of the first mechanical samples produced with this technology are shown in Fig. 9.

6. Summary

The DEPFET is a promising candidate to fulfill the challenging detector requirements of future high energy physics experiments, e.g. the TESLA vertex detector. It offers an excellent low noise performance at room temperature. Thus the DEPFET has the potential to achieve a good spatial resolution and a fast readout speed even on a thinned detector substrate. The overall requirement of a minimum material budget is addressed

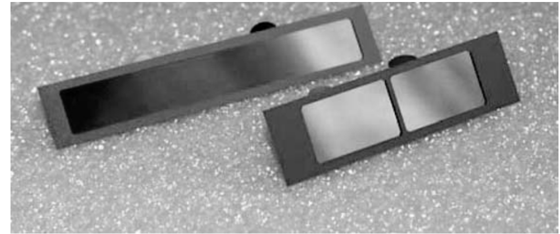

Fig. 9. First results of the thinning technology development—mechanical samples. The size of the upper part is $800 \times 104\,mm^2$.

by an intrinsically low power consumption, thereby saving material for cooling structures. At the MPI Semiconductor Laboratory, a new MOS based technology on 150 mm wafer has been developed to produce large detector arrays.

Linearly shaped DEPFETs of a size of about $25 \times 25\,\mu m^2$ can be made by using two polysilicon layers. As a detector pixel cell consists of only one single DEPFET transistor it can be produced by rather large lithographic structures with minimum size of 2 μm. Therefore the yield problem occurring especially in large area detectors is expected to be relaxed. Technology development and detector design based on two and three-dimensional processes and device simulations demonstrating the operation and the technological feasibility of DEPFET arrays. The first production run has been started. A thinning technology based on direct wafer bonding is proposed. Mechanical samples with 50 μm thinned regions were fabricated successfully.

Acknowledgements

We would like to thank K.E. Ehwald and B. Heinemann from IHP, Frankfurt/Oder for helpful discussions and suggestions. The simulation software POSEIDON was developed by A. Castoldi, E. Gatti and P. Rehak within the INFN-RIMAX project.

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