Lock-in thermography and nonuniformity modeling of thin-film CdTe solar cells

Diana Shvydka

Department of Physics and Astronomy, University of Toledo, Toledo, Ohio 43606

J. P. Rakotoninaia and O. Breitenstein

Max-Planck-Institut für Mikrostrukturphysik, Weinberg 2, D-06120 Halle, Germany

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We present the lock-in thermography study of thin-film CdTe/CdS solar cells. Several major features of thermal signal are identified, such as much higher intensity for cells under illumination, considerable inhomogeneity, and a bright contour line corresponding to the higher intensity at the cell edge. Light soak stress is shown to increase the device lateral nonuniformity. We model the solar cell as a two-dimensional system of random diodes connected in parallel through a resistive electrode. The simulated current distribution maps are consistent with the thermography data. © 2004 American Institute of Physics. [DOI: 10.1063/1.1645322]

In recent years, lateral nonuniformity has become an important issue in thin film photovoltaic research, in particular because of the urgent need to scale small laboratory-prepared devices up to large commercially manufactured modules. Significant variation in photovoltaic parameters between nominally identical devices is one practically important consequence of nonuniformity. Since individual cells in a module are interconnected, occasional bad parts affect the whole device performance and stability. The nonuniformity appears on different scales as detected by different mapping techniques, such as surface photovoltage, optical beam and electron-beam-induced current, recombination lifetime, photoluminescence, etc. (see Refs. 1 and 2, and references therein).

Lock-in thermography has proven a valuable technique for nonuniformity diagnostics in crystalline and multicrystalline solar cells. It utilizes ac IR imaging of a device, where the temperature is affected by an external ac voltage of the same (lock-in) frequency. The thermography maps thus represent the current distributions. Surprisingly, this technique remained relatively modern to the thin-film technology, where nonuniformity effects are most detrimental. In this letter we present the IR lock-in thermography data and corresponding modeling for polycrystalline thin-film CdTe/CdS solar cells.

For this study, devices were prepared by three different deposition techniques: radio-frequency sputtering, vapor transport deposition (VTD), and close-space sublimation. In all cases, a layer of CdS followed by a CdTe layer was deposited on commercially available SnO2-coated glass substrate. The latter transparent conductive oxide (TCO) served as a front electrode. After deposition, the samples were submitted to a standard anneal in the presence of CdCl2 vapor, which generally leads to improved electrical characteristics. Finally, a metal layer was deposited to form the back contact to CdTe. Devices were measured as prepared and then after 56 days of light soak stress, conducted at open circuit under one sun illumination, 65 °C. Such stress is often used to study the device efficiency degradation.

The lock-in thermography was carried out using a commercial TDL 384 M “Lock-in” thermography system by Thermosensorik GmbH (Erlangen). Following the standard technique several samples of each lot have been measured at a lock-in frequency of 3 Hz in two modes: (a) forward bias pulses (0 to 0.8–1 V) under laboratory light condition (nominally, in the dark), and (b) forward bias pulses (0 to 0.8–1 V) under continuous illumination. Different forward biases were used in order to have comparable forward currents, leading to comparable thermographic signals. Cells were imaged from the back contact side, since the substrate was not transparent to the IR light of 3–5 μm used. The sample was contacted with a pin with a small piece of nickel foil placed below to avoid scratching. Since the metallized area had a low IR emissivity, the phase image, which is independent from the IR emissivity, was also examined and correlated with the amplitude image variations. In some cases the IR emissivity was increased by covering the surface with a black paint.

Shown in Fig. 1 are amplitude images scaled up to a maximum temperature modulation amplitude of 3 mK (the contacting probe is visible in the lower right corner of each map). Figures 1(a) and 1(b) show the typical maps obtained in the dark and under illumination, respectively. Generally, we observed much lower thermal signal in the dark. While this particular device was prepared by VTD technique, we did not see significant differences in the observed features between this and other cells. In most cases the edge of the cell showed a larger thermal signal (bright contour line), even after covering the cell with a black paint; the phase signal indicated the same.

Figure 1(c) shows the same cell measured under illumination after light soak stress. The open circuit voltage for this cell changed from 773 mV before to 317 mV after the stress. The thermography signal intensity typically increased by a factor of ~3 after the stress, becoming more nonuniform. This map also shows one very bright spot close to the cell center, which we identify as a nonohmic shunt, not visible...
under reverse bias. The size of this spot corresponds to the characteristic thermal length.\(^4\) Some of the cells developed true shunts in the process of light-induced degradation. The bright edge line width increased after the light soak.

Summarizing, several typical features are identifiable: (1) considerable signal inhomogeneity, increasing after light soak stress (consistent with the result in Ref. 6), and pointing to lateral inhomogeneities in the current flow; (2) bright contour line corresponding to higher signal at the cell edge; (3) rear spots of very high signal, in most cases not visible under reverse bias; and (4) dark area off the contact.

We attribute the above features to spatial variations in the device local characteristics. This is reflected in the model of random diodes connected in parallel through a resistive electrode,\(^1,2\) as illustrated in Fig. 2 (see also Refs. 7 and 8 for multicrystalline Si solar cells). Series resistors qualitatively represent the back barrier (back diode) effect, attributed to the CdTe-metal interface.\(^10,11\) The back barrier is suppressed beyond the contact.

We used the equivalent circuit in Fig. 2 for numerical simulations with the following input parameters: open-circuit voltage \(V_{oc}\), series resistance \(R_s\), shunt resistance \(R_{sh}\) on each diode, and sheet resistance of the most resistive layer \(R_s\) (TCO for metallized area, or semiconductor sheet resistance for a contact-free area), bias voltage \(V\) applied at the edge of a cell as a boundary condition. Given the latter parameters and the nonideality factor, the standard diode equation\(^12\) was used to calculate the current in each of the units.

To simulate a nonuniform system, the individual diode parameters, \(V_{oc}\), \(R_s\), etc., were randomly generated to obey either Gaussian or uniform distributions with the typically observed\(^1,2\) respective averages and dispersions. The electric potential and current distributions in the circuit were then calculated by numerically solving a set of Kirchhoff’s equations.

For this study we simulated a two-dimensional system of 30×30 diodes. The input parameters were chosen to correctly predict the typically observed current-voltage characteristics. The effects of disorder were modelled by the uniform \(V_{oc}\) distribution with relative mean-square-root fluctuation of 10%, and the Gaussian \(R_s\) distribution with relative standard deviation of 25%. The Gaussian distribution for \(R_s\) was chosen to allow for rare spots of negligibly small \(R_s\) that mimic the region of high back barrier transparency.

We have chosen the parameter distribution corresponding to two contacts separated by a contact-free area. The resulting map of currents is shown in Fig. 3(a). Similar to the thermography maps, the current distribution in contacts is inhomogeneous. We also observe a bright line corresponding to high current value near contact edges followed by a dark region of zero current from contact-free area. Physically, the bright edge feature is due to the higher forward current density through a narrow region bordering with the contact. This region provides a low-resistance pathway where the back barrier is absent and \(R_s = 0\). A bright spot in the upper contact represents an abnormally weak diode with \(V_{oc}\) three times lower than the average value. Shown in Figs. 3(b) and 3(c) are two other features predicted by our modeling: a region of high back barrier transparency in the back barrier (\(R_s = 0\)) and a combination of the region of high back barrier transparency with a weak (low \(V_{oc}\)) diode. The latter serves as a strong shunt that robs current from a large surrounding area.

To further explain the bright edge feature, we note that the current decay beyond the metallized region occurs in the
under ambient illumination, we estimate $l=0.3$ mm, consistent with our measurements [Figs. 1(a) and 1(b)]. Since $R_{oc}$ typically increases after the light soak stress, Eq. (1) also offers an explanation for the observed increase in the bright line width after the degradation [Fig. 1(c)].

In conclusion, we present the lock-in thermography data and related random-diode model simulation for CdTe/CdS solar cells. We identify the main observed features and show that all of them can be simulated in the framework of our model. Our results demonstrate that IR lock-in thermography is a valuable technique for thin film solar cell diagnostic, revealing nonuniformities in the device back contact and main junction. One more specific result of this study is that the degree of nonuniformity correlates with the device deterioration usually observed under light soak stress.

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5 www.thermosensorik.de.