Fundamental issues in wafer bonding

U. Gösele,[a),b)] Y. Bluhm, G. Kästner, P. Kopperschmidt, G. Kräuter, R. Scholz,
A. Schumacher, St. Senz, and Q.-Y. Tong[b),c)]
Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany

L.-J. Huang, Y.-L. Chao, and T. H. Lee
Wafer Bonding Laboratory, School of Engineering, Duke University, Durham, North Carolina 27708-0300

Semiconductor wafer bonding has increasingly become a technology of choice for materials integration in microelectronics, optoelectronics, and microelectromechanical systems. The present overview concentrates on some basic issues associated with wafer bonding such as the reactions at the bonding interface during hydrophobic and hydrophilic wafer bonding, as well as during ultrahigh vacuum bonding. Mechanisms of hydrogen-implantation induced layer splitting (''smart-cut'' and ''smarter-cut'' approaches) are also considered. Finally, recent developments in the area of so-called ''compliant universal substrates'' based on twist wafer bonding are discussed. © *1999 American Vacuum Society.* [S0734-2101(99)06504-5]

I. INTRODUCTION

''Wafer bonding'' refers to the phenomenon that mirror-polished, flat, and clean wafers of almost any material, when brought into contact at room temperature, are locally attracted to each other by van der Waals forces and adhere or ''bond'' to each other. Historically, probably the first report on the sticking of flat glass plates can be found in a 1638 book by Galileo Galilei.[1] Later on, this phenomenon was empirically known and partly used for optically polished pieces of materials and was first scientifically investigated for polished pieces of quartz glass by Lord Rayleigh[2] in 1936. In the sixties and seventies, this adherence phenomena was used for some isolated applications involving glass[3] by van Bueren *et al.* or III–V compound wafers[4] by Antypas and Edgecumbe. In the eighties, almost simultaneously researchers at Toshiba[5] and IBM[6] used this room temperature adhesion phenomenon followed by an appropriate heating step for silicon wafers in order to replace epitaxial growth of thick silicon wafers or to fabricate silicon-on-insulator (SOI) structures, respectively. Shortly afterwards, the bonding of structured silicon wafers was applied for the fabrication of micromachined pressure sensors and termed ''silicon fusion bonding.''[7] In the meantime, wafer bonding has been applied to all kinds of materials combinations involving silicon or other materials.[8] The wide availability of chemo-mechanical polishing in integrated circuit fabrication and of a variety of precision thinning approaches has led to a widespread and diverse use of wafer bonding. The application areas range from microelectronic devices based on SOI material to power devices, high voltage devices, optoelectronic devices based on III–V compounds,[9–12] nonlinear optics devices,[13] and microelectromechanical systems[14] including pressure and acceleration sensors. Although wafer bonding can be applied as a simple and elegant method to join equal or different materials, one of its main advantages appears to be the possibility to fabricate single-crystalline layers on top of substrates which may be either amorphous, poly-crystalline, or single crystalline with a large lattice mismatch and thus cannot be used for epitaxial growth of the desired single-crystalline layers.

In the present overview, we will concentrate on selected fundamental materials science issues associated with wafer bonding. Section II starts with processes occurring during room temperature silicon bonding including bonding under ultrahigh vacuum (UHV) conditions. Section III will deal with reactions which occur at the bonding interface during a subsequent heating step. In Sec. IV we will describe thinning procedures with special emphasis on hydrogen-implantation induced layer splitting (''smart-cut'' and ''smarter-cut'') for silicon and other materials. Finally, in Sec. V we will highlight recent progress in the understanding of so-called ''compliant universal substrates'' based on twist wafer bonding. Since we will not cover all areas of wafer bonding and its applications, for a more extensive treatment of this field we refer the reader to recent conference proceedings,[15–18] review articles,[19–30] a special 1995 issue of the Philips Journal of Research[31] and a book[32] on this subject.

II. ROOM TEMPERATURE PROCESSES

A. General remarks

Wafer bonding requires clean and mirror-polished surfaces which may be chemically conditioned before bonding. In the case of silicon wafer bonding, three principle kinds of surface conditioning are used: (i) hydrophilic surfaces which usually consist of an oxide layer (native oxide or thermally grown oxide) to which water molecules are attached via intermediate OH-groups, (ii) hydrophobic surfaces which consist of hydrogen saturated silicon surfaces obtained by an HF-dip removing any oxide layer, and (iii) clean silicon surfaces without adsorbates which may be realized only under

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[a)]Electronic mail: goesele@mpi-halle.de
[b)]Also at: School of Engineering, Duke University, Durham, North Carolina 27708-0300.
[c)]Present address: Research Triangle Institute, Research Triangle Park, North Carolina 27709.
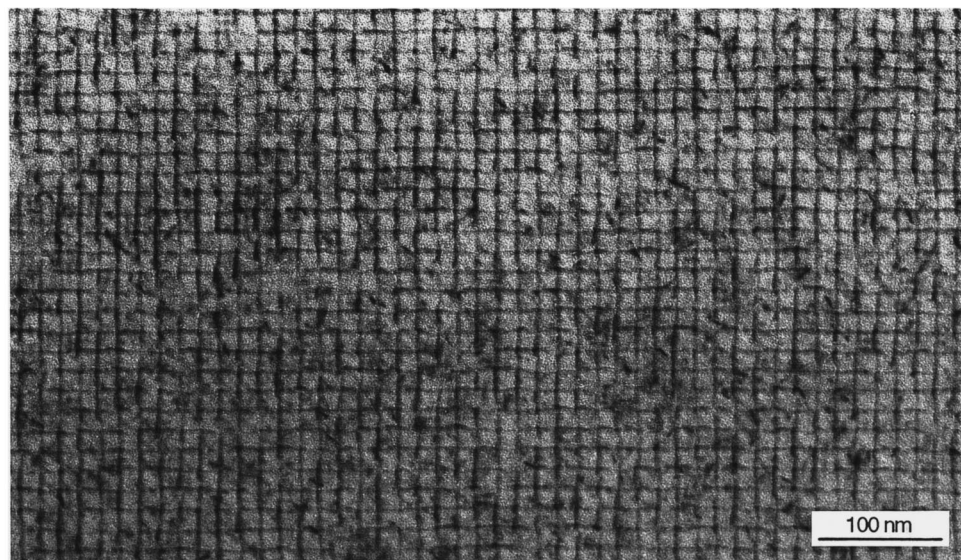
FIG. 1. Plan view TEM picture of screw dislocation network at interface of two (100) silicon wafers bonded at room temperature under UHV conditions without any subsequent annealing treatment (Ref. 44).

UHV conditions. In the following, we will discuss some specific questions associated with the bonding process at room temperature using the example of silicon.

B. Hydrophilic and hydrophobic bonding

For hydrophobic and hydrophilic silicon wafers, the contacting of the two wafers is usually performed at room temperature in ambient atmosphere. In order to avoid particles between the wafers, which would lead to unbonded areas (often termed interface bubbles or voids) the contacting has to be performed in a clean room of class ten or better or in a ''micro-cleanroom.'' A micro-cleanroom[33] is a centrifuge-based device specifically designed to avoid particles between the surfaces of wafers to be bonded. After contacting the wafers, the actual bonding starts at one location (typically after initiation by applying locally a slight pressure). The bonded area then spreads over the whole area within a few seconds. It was shown that the speed of the lateral spreading of the bonded area is independent of wafer thickness and distance to the wafer rim but increases with decreasing pressure of the outside atmosphere and is thus associated with pressing gas out from a region close to the edge of the bonded region.[34,35] In agreement with this conclusion, the lateral bonding speed under UHV conditions is too fast to be measured with an infrared camera.

Whether two wafers actually bond over the entire area, only partially, or not at all depends on the bonding energy at room temperature and the roughness and waviness of the two wafers. The bonding energy may be characterized by the energy γ per surface area required to separate the bonded wafers by the so-called crack-opening method first described by Maszara *et al.*[36] Directly after room temperature bonding, the adhesion between the two wafers is determined by van der Waals interactions or hydrogen bridge bonds and one or two orders of magnitude lower than typical for covalent bonding. The surface energy γ is typically around 100 mJ/m^2 for hydrophilic surfaces and around 20 mJ/m^2 for (hydrogen

covered) hydrophobic silicon surfaces generated by an HF dip.[37,38] Nowadays, it is also possible to calculate at least approximately whether wafers with a certain waviness and roughness will bond or not.[25,39–41] In agreement with experimental observations, the theoretical results indicate that the wafers do not have to be atomically flat to bond and a certain wafer bow can also be tolerated.

C. UHV bonding

For most practical applications a higher bond energy is required than obtained after room temperature hydrophilic or hydrophobic bonding. Such an increase may be accomplished by an appropriate heating step associated with chemical reactions which will be discussed in detail in Sec. III. This heating step is frequently performed at temperatures as high as 1100 °C in the case of silicon. An attractive possibility to reach the full bonding energy directly at the room temperature bonding step consists in contacting two silicon surfaces free of adsorbates under UHV conditions. Molecular dynamics simulations showed that, although the silicon surfaces are reconstructed under these circumstances, the reconstructed bonds will break up at room temperature when the surfaces get close enough to each other.[42,43] The simulations also predict that atomic and diatomic surface steps will not prevent spontaneous covalent bonding. The actual experimental results for commercial 4 in. (100) silicon wafers are in agreement with these predictions.[42,44] Figure 1 shows a plan view of the interface with the corresponding square array of screw dislocations accommodating a small twist angle between the two silicon wafers. Mechanical testing of the UHV bonded silicon wafers also confirms the covalent nature of the bonding at the interface. Covalent bonding has also been accomplished for GaAs pieces[45] at room temperature under UHV conditions although only for small (1×1 cm) pieces and under some mechanical pressure. Other successful attempts for UHV bonding[46,47] were performed at elevated temperatures.
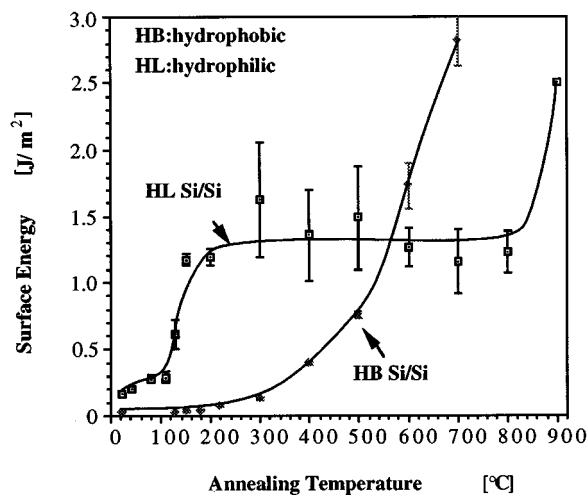
FIG. 2. Saturation values of surface or bonding energy measured by the crack-opening method as a function of temperature after long-time heat treatments (up to 100 h) (Ref. 29).

III. CHEMICAL REACTIONS AT BONDING INTERFACES

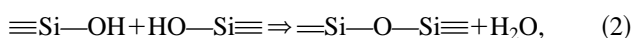### A. Silicon/silicon bonding

As mentioned earlier, the bonding energy associated with hydrophilic or hydrophobic wafer bonding at room temperature is too low for most applications. Therefore, a subsequent heating step is added which causes chemical reactions at the interface leading to a higher bonding energy. The increase of the surface energy as a function of temperature for long time annealing to a saturation value is shown in Fig. 2 after bonding in air at room temperature.[29] A clear difference between hydrophobic and hydrophilic bonding can be seen. The reactions at the bonding interface can conveniently be investigated by multiple internal reflection spectroscopy which also allows one to distinguish different reaction behavior of hydrophobic wafer surfaces of different crystallographic orientations. For details the reader is referred to the articles[48–50] by the group of Chabal.

For hydrophobically bonded wafers the reaction during heating consists of sequential hydrogen desorption (depending on the specific bonding configuration) and silicon-silicon covalent bond formation across the interface according to

$$\equiv\!Si\!-\!H + H\!-\!Si\!\equiv \;\Rightarrow\; \equiv\!Si\!-\!Si\!\equiv + H_2. \tag{1}$$
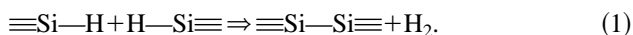
At temperatures up to about 600 °C the hydrogen diffuses along the bonding interface rather than diffusing into the silicon.

In the case of hydrophilic wafer bonding the end result, namely the generation of molecular hydrogen, is the same but there are intermediate steps involved. At the interface, initially there exists molecular water adsorbed on hydrophilic oxides. Molecular water will also come partly from the reaction

$$\equiv\!Si\!-\!OH + HO\!-\!Si\!\equiv \;\Rightarrow\; \equiv\!Si\!-\!O\!-\!Si\!\equiv + H_2O, \tag{2}$$

which starts to form strong covalent bonds across the bonding interface at temperatures above about 120 °C. Molecular water will oxidize the surrounding crystalline silicon and form molecular hydrogen via the reaction

$$Si + 2H_2O \Rightarrow SiO_2 + 2H_2. \tag{3}$$

The hydrogen development at the interface was measured rather directly by bonding structured silicon wafers containing cavities of the same size but different area densities in different parts of the wafers.[51,52] The cavities were deep enough to leave silicon membranes, which allowed the investigation of the pressure increase in the cavities after bonding in high vacuum at room temperature and subsequent temperature treatments. If hydrogen gas develops at the interface during annealing and diffuses along the interface, it is expected that the cavities with the lower area density (and consequently the larger surrounding bonding area per cavity) should show a larger pressure increase. This is actually the case for both hydrophobic and hydrophilic wafers. Opening the cavities in a UHV system allowed the analysis of the gas in the cavities, which turned out to consist mainly of hydrogen, as expected from reactions (1) and (2), and a small percentage of hydrocarbons.

A thin oxide favors reaction (3) and therefore the formation of strong bonds for a given relatively low temperature as compared to the case of much thicker thermal oxides through which the water molecules have to diffuse before getting to the silicon. On the other hand, the hydrogen molecules resulting from reaction (2) cannot appreciably be dissolved in the silicon and therefore, generate a high gas pressure at the interface. This pressure, which may lead to formation of interface bubbles or weakening of the bonding, decreases with increasing oxide thickness (since the hydrogen can be dissolved in the oxide.) Therefore, for strong and high quality bonding a combination of a very thin oxide [which favors getting rid of the water via reaction (3)] and a thick oxide (which reduces the pressure at the interface) appears to be most favorable,[53] as was found experimentally.[54]

For both hydrophilic and hydrophobic bonding a gas pressure will develop in cavities even if the room temperature bonding is performed under high vacuum conditions. For absolute pressure sensors it is desirable to avoid any gas development at all. Bonding under UHV conditions, in principle, should allow this goal to be achieved but has not yet been verified experimentally.

Since reactions (2) and (3) can proceed already at temperatures slightly above 100 °C, it is astonishing that the surface energy for hydrophilic bonding at low to intermediate temperatures shown in Fig. 2 does reach only about a third to one half of the full value for covalent bonding. In the meantime, it appears likely that nitrogen trapped at the interface during room temperature bonding in air prevents reaction (2) to proceed to completion. Room temperature bonding under low vacuum conditions[55] shows a drastic increase of the plateau value for the surface energy at low temperatures (Fig. 3). This simple procedure allows one to obtain high bonding
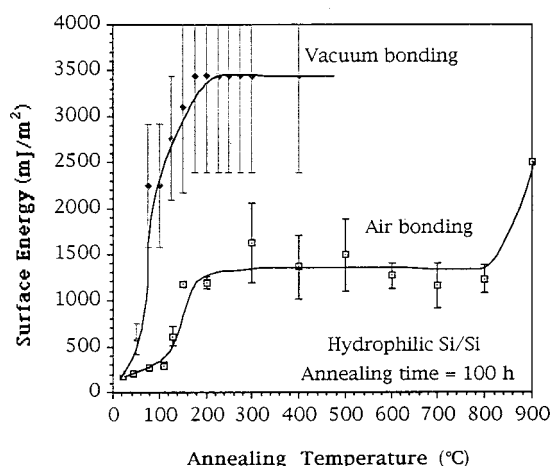
FIG. 3. Saturation values of surface energy for low vacuum or air bonded silicon wafers as a function of temperature after long-time heat treatments (up to 100 h) (Ref. 55).
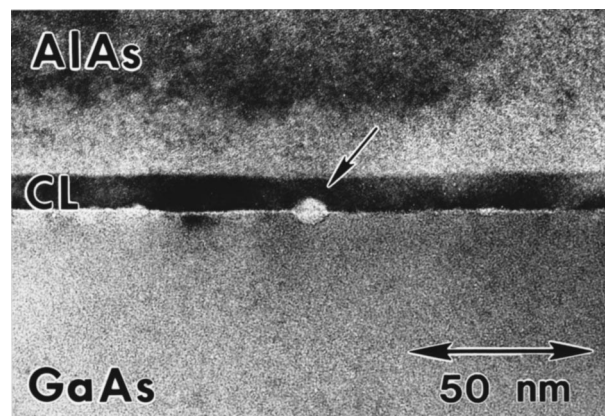

FIG. 4. Cross-sectional TEM picture of bonded GaAs/GaAs wafers showing an interface defect indicated by an arrow. CL stands in short for an epitaxially grown compliant GaAs layer (Ref. 61).

energies at temperatures below 200 °C so that temperature sensitive parts such as metallization layers will not be adversely affected.

We will not discuss the promising low temperature bonding approach based on a plasma treatment of the silicon surfaces.[56-58] In this case, the detailed reactions are not yet understood and are presently under investigation by multiple internal reflection spectroscopy at MPI Halle.

B. General materials combinations

Most materials, if properly polished and with their surfaces properly conditioned, do adhere to each other at room temperature and can thus be used for wafer bonding approaches as has been shown by the group of Haisma[8] at Philips. Besides the usual requirements concerning roughness and avoiding particles, in each case one also has to consider the chemical reactions proceeding at the interface. This area is relatively poorly investigated and understood. For III–V compounds contacting and wafer bonding frequently occurs at elevated temperatures (typically around 500–600 °C) in hydrogen and often under the application of an outside force.[27,28] The hydrogen is supposed to clean off the native oxide on the wafer surfaces. We observed by cross-sectional and plan view transmission electron microscopy that GaAs wafers bonded to other GaAs wafers, to silicon, or to sapphire show nanometer sized defects at the interface.[59-61] An example is shown in Fig. 4 for a GaAs wafer bonded to a GaAs wafer covered with an epitaxial AlAs layer and a 10 nm thick GaAs layer.[61] Presently, it is not clear whether these interface defects are mainly voids as a result of a local rearrangement of the surface roughness[62] or rather the result of a chemical reaction between remaining water molecules and the GaAs. These interface defects may have an essential impact on the realization of so-called compliant universal substrates discussed in Sec. V. It is not

known to the authors whether these interface defects may completely be avoided by proper cleaning and processing conditions.

IV. HYDROGEN-IMPLANTATION INDUCED LAYER SPLITTING

Depending on the specific application, thinning of one of the bonded wafers down to a thickness between about 10 nm to some micrometers is required. From the many different approaches such as precision polishing, the use of etch-stop or polishing/grinding stop layers, we will discuss here only an especially elegant procedure that has been suggested by Bruel and termed smart-cut.[63,64] It is based on hydrogen implantation before bonding which leads to the splitting of silicon wafers along hydrogen-filled microcracks induced by the precipitation of the implanted hydrogen during a heating step after bonding. The process is also known as hydrogen-implantation induced ''layer splitting,'' ''exfoliation,'' ''delamination,'' or ''ion-cut.''

One main advantage of this procedure, which also allows a thickness variation in the 10 nm range, is that split wafers may be re-used (after some soft polishing, which is also required for the transferred layer) since its thickness has changed only by about a micrometer or less. Co-implantation of a much lower dose of boron allows one to decrease the temperature and/or time of splitting considerably (smarter-cut).[65] Lower temperature layer splitting is most important for bonding materials of different coefficients of thermal expansion such as silicon and quartz glass. Implantation of silicon at higher temperatures than room temperatures may lead to fewer defects and will also allow splitting at lower temperatures. A combination of low dose boron implantation and high temperature hydrogen implantation allows one to considerably reduce the minimum dose of hydrogen required to perform layer splitting.[66] A similar reduction of the minimum required dose may also be accomplished by helium and hydrogen co-implantation.[67]

If hydrogen-implanted wafers are annealed without bonding, surface blisters will develop. These blisters will finally
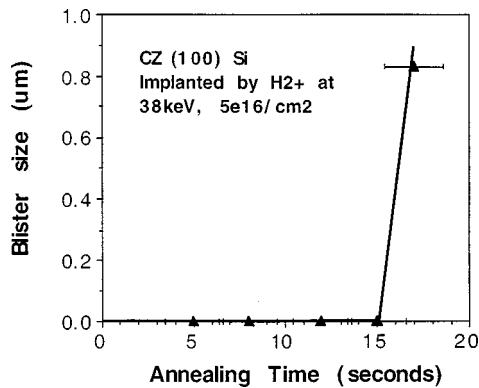
FIG. 5. Size of surface blisters in hydrogen implanted silicon as a function of annealing time at 350 °C as observed by AFM (Ref. 69).

FIG. 7. Same as Fig. 8 for InP implanted at around 200 °C (Ref. 73).

break and ''flaking'' will occur as has been known as an undesirable side effect of hydrogen (and helium) implantation for many years.[68] Observing these surface blisters is a convenient way of investigating the hydrogen agglomeration process as a function of implantation temperature, implantation dose and energy, annealing temperature and time, and crystallographic orientation. We have observed experimentally, that the surface blisters suddenly develop after a specific annealing time which we called blistering time. By atomic force microscopy (AFM) we could show that this effect is not due to the limited resolution of the optical observation method but actually a popping up of the blisters at a specific time (Fig. 5).[69] Therefore, we may assume that the micro-cracks first grow laterally in a closed form before popping up after reaching a critical size. The critical size depends on the layer thickness and the hydrogen implantation dose. This initial lateral growth of micro-cracks allows one to pre-anneal hydrogen implanted unbonded wafers to a time just before the popping up occurs. Then the wafers can be bonded and the actual splitting can be performed at lower

temperatures and/or shorter times than required without pre-annealing.[65]

Layer splitting by hydrogen implantation and wafer bonding is especially interesting for expensive materials such as single crystalline SiC,[70,71] diamond,[71] GaAs,[72,73] InP,[73] or GaN[73] for which the smart-cut procedure also works. In Fig. 6, the annealing time to observe surface blisters after hydrogen implantation in Si, Ge, and SiC as a function of reciprocal temperature is shown. It is important to note that microcracks may develop only for certain implantation temperatures which may not include room temperature. For too low a temperature, implantation will generate too much lattice damage to allow sufficient hydrogen agglomeration. For too high a temperature, hydrogen is already mobile during the implantation process and will move out of the implanted region. For III–V compounds, the temperature window for hydrogen implantation turns out to be quite narrow. Some results are shown for developing of blisters for InP in Fig. 7. Examples of transmission electron microscopy (TEM) or scanning electron microscopy (SEM) micrographs of blis-
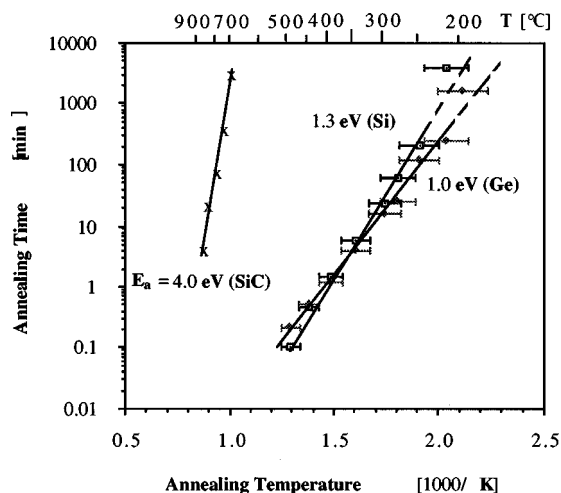

FIG. 6. Annealing time required to observe surface blisters in hydrogen implanted Si, Ge, and SiC as a function of inverse absolute temperature (Ref. 29).
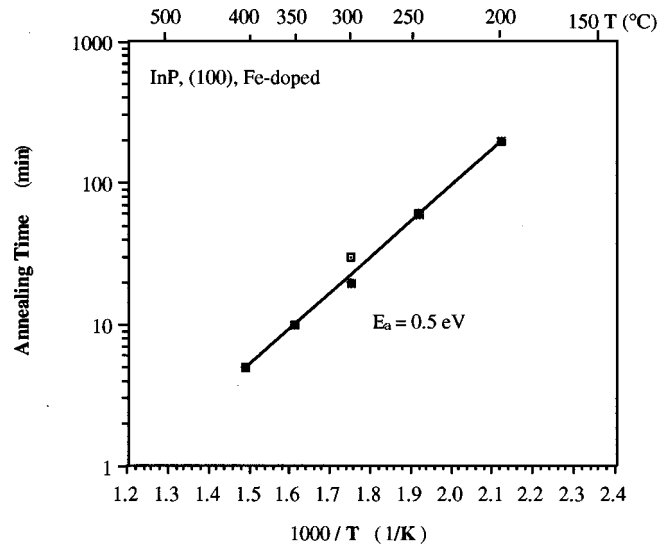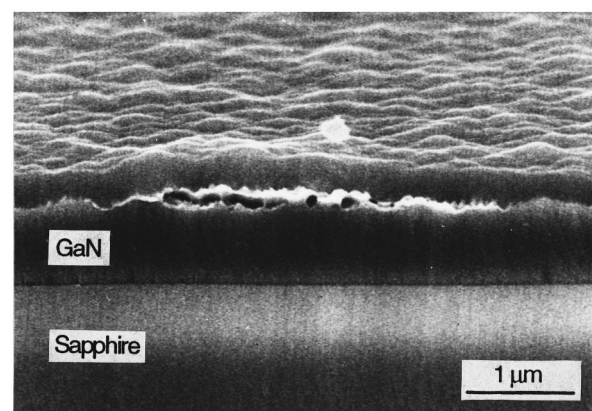

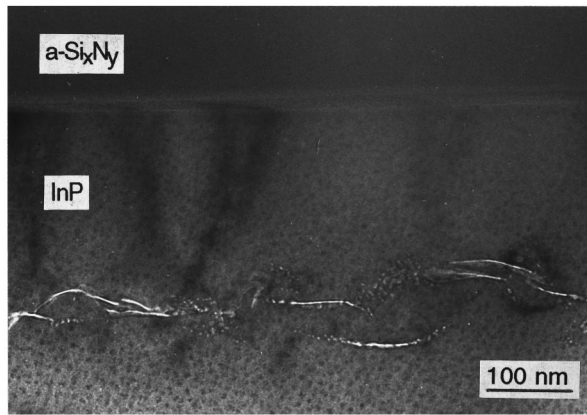FIG. 8. SEM picture of hydrogen-implantation induced blisters in GaN (Ref. 73).

FIG. 9. Cross-sectional TEM picture of hydrogen-implantation induced microcracks in InP (Ref. 73).

ters developing in hydrogen implanted GaN (grown on a sapphire wafer), InP, and GaAs are shown in Figs. 8–10, respectively. First results indicate that complex oxides such as sapphire or LaAlO$_3$ also show the blistering and splitting effect. Based on earlier studies[68] it is expected that GaP and most other materials should be susceptible to this layer splitting process, provided that appropriate processing conditions are used.

Repeated transfer of thin single crystalline layers of expensive materials onto appropriate inexpensive substrates (e.g., single crystalline SiC onto polycrystalline SiC) could allow a large decrease in price of these materials and consequently to more widespread and economic usage. Hydrogen implantation induced layer splitting may also enable further advances in three-dimensional integration of microelectronic devices and possible integration with opto-electronics.

V. COMPLIANT UNIVERSAL SUBSTRATES

Hetero-epitaxial growth of single crystalline layers on a substrate with a different lattice constant leads to the incorporation of misfit dislocations if the film exceeds a critical thickness, which depends on the lattice misfit of the two materials. The generation of misfit dislocations is generally associated with a high density of threading dislocations in the epitaxially grown layer. It has always been a dream to have a ''magic'' substrate available, which would allow one to avoid the generation of misfit dislocations or at least that of threading dislocations. Theoretically, it was shown that epitaxial growth on an extremely thin substrate which would

FIG. 10. Cross-sectional TEM picture of hydrogen-implantation induced micro-cracks in GaAs (Ref. 73).
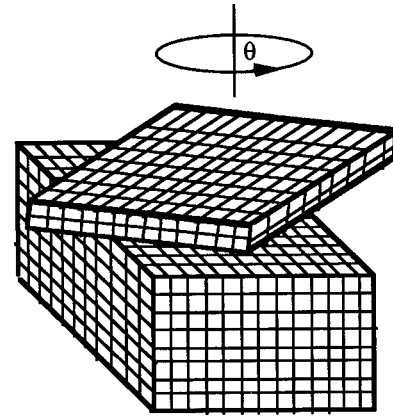

FIG. 11. Schematic of twist bonded compliant substrate (Ref. 29).

always remain below its critical thickness would comply to the growing film and no misfit dislocation should be generated.[74,75] Although this has been shown to work also experimentally,[76] such thin films as substrates are not practical. Recently, Lo and co-workers[77–79] at Cornell University have fixed a very thin layer of (100) GaAs on a (100) GaAs substrate rotated by a certain twist angle. The fabrication was accomplished by twist wafer bonding of two GaAs wafers (based on earlier bonding approaches by Liau and Mull)[80] one of which contained an epitaxial AlGaAs etch-stop layer followed by a thin (about 3–10 nm) GaAs layer and subsequent back-etching. The resulting structure is schematically shown in Fig. 11. Growth of misfitting III–V compounds (InGaAs and InSb) on this thin GaAs layer bonded on the GaAs handle wafer showed a drastically reduced density of threading dislocations.[77,78,81] The compliant universal substrates, as the material was called by Lo and co-workers, created an enormous interest in the scientific community.[82,83] Recently, Lo and Zhu[82] have demonstrated that the concept can be extended to twist bonded silicon films on silicon. Presently, it is unclear how such a compliant universal substrate would actually work. A potential threading dislocation
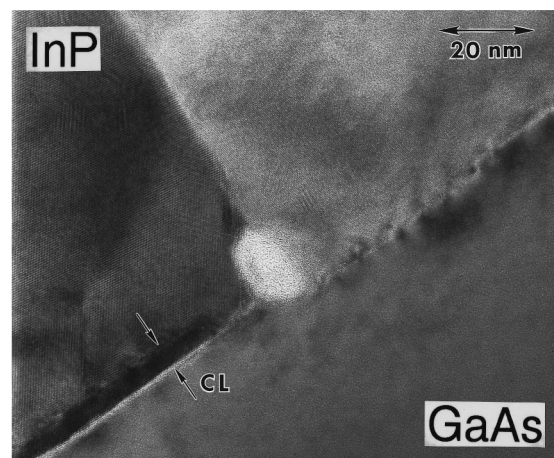

FIG. 12. Cross-sectional TEM of two InP grains epitaxially grown on a twist bonded compliant GaAs substrate with pin holes due to bonding defects (Ref. 61).

annihilation mechanism based on the existence of a square grid of screw dislocations at the twist bonding interface has been suggested by Kästner *et al.*[84] In our own experiments in which we tried to confirm the Cornell results we also got hetero-epitaxial layers free of threading dislocations.[61] However, it turned out that our twist bonded GaAs layer contained a high density of pin holes most likely due to the nanometer-sized defects at the bonding interface shown in Fig. 4. As a consequence, our hetero-epitaxially grown layer consisted of 0.1—several micrometer sized grains with either the orientation of the twist bonded GaAs film or the orientation of the GaAs handle wafer in the areas where pin holes existed. The grains were fully relaxed and the threading dislocations had moved to the grain boundaries. An example of two differently oriented grains of InP grown on the GaAs twist bonded layer is shown in Fig. 12. Naturally, the question arises whether the twist bonded GaAs films in the case of the Cornell experiments also contained pin holes or whether they were continuous and the observed reduced dislocation densities are actually due to a ''compliance'' based e.g., on the mechanism suggested by Kästner *et al.*[84] This question cannot be answered with any certainty. Clearly further experiments are needed in this fascinating area.

ACKNOWLEDGMENTS

[1] G. Galilei, *Discorsi E Dimostrazioni Matematiche* (1638), reprinted, edited by Le Opere (Mailand, 1938), Vol. 2.
[2] Lord Rayleigh, Proc. Phys. Soc. London **156**, 326 (1936).
[3] H. G. van Bueren, J. Haisma, and H. de Lang, Phys. Lett. **2**, 340 (1962).
[4] G. A. Antypas and J. Edgecumbe, Appl. Phys. Lett. **26**, 371 (1974).
[5] M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, J. Appl. Phys. **60**, 2987 (1986).
[6] J. B. Lasky, Appl. Phys. Lett. **48**, 78 (1986).
[7] K. Petersen, Proceedings of IEEE Solid State Sensor Conference, Hilton Head, SC, 1988.
[8] J. Haisma, B. A. C. M. Spierings, U. K. P. Biermann, and A. A. v. Gorkum, Appl. Opt. **33**, 1154 (1994).
[9] R. J. Ram, L. Yang, K. Nauka, M. Houng, M. Ludowise, D. E. Mars, J. J. Dudley, and S. Y. Wang, Appl. Phys. Lett. **62**, 2474 (1993).
[10] D. I. Babic, J. J. Dudley, K. Streubel, R. P. Mirin, J. E. Bowers, and E. Hu, Appl. Phys. Lett. **66**, 1030 (1995).
[11] D. I. Babic, J. E. Bowers, E. L. Hu, L. Yang, and K. Carey, Int. J. High Speed Electron. Syst. **8**, 357 (1997).
[12] D. A. Vanderwater, I.-H. Tan, G. E. Höfler, D. C. Defevere, and F. A. Kish, Proc. IEEE **85**, 1961 (1995).
[13] L. Gordon, G. L. Woods, R. C. Eckhardt, R. R. Route, R. S. Feigelson, M. M. Fejer, and R. L. Byer, Electron. Lett. **29**, 1942 (1993).
[14] M. A. Schmidt, Proc. IEEE **86**, 1575 (1998).
[15] *First International Symposium Semiconductor Wafer Bonding: Science, Technology and Applications*, Electrochemical Society Proceedings, Vol. 92–7, edited by U. Gösele, J. Haisma, M. Schmidt, and T. Abe (Electrochemical Society, Pennington, NJ, 1992).
[16] *Second International Symposium Semiconductor Wafer Bonding: Science, Technology and Applications*, Electrochemical Society Proceedings, Vol. 93–29, edited by H. Baumgart, Ch. Hunt, M. Schmidt, and T. Abe (Electrochemical Society, Pennington, NJ, 1993).
[17] *Third International Symposium Semiconductor Wafer Bonding: Science, Technology and Applications*, Electrochemical Society Proceedings, Vol. 95–7, edited by H. Baumgart, Ch. Hunt, S. Iyer, U. Gösele, and T. Abe (Electrochemical Society, Pennington, NJ, 1995).
[18] *Fourth International Symposium Semiconductor Wafer Bonding: Science, Technology and Applications*, Electrochemical Society Proceedings, Vol. 97–36, edited by U. Gösele, H. Baumgart, Ch. Hunt, and T. Abe (Electrochemical Society, Pennington, NJ, 1998).
[19] J. Haisma, B. A. C. M. Spierings, U. K. P. Biermann, and J. A. Pals, Jpn. J. Appl. Phys., Part 1 **28**, 1426 (1989).
[20] P. W. Barth, Sens. Actuators A **21–23**, 919 (1990).
[21] W. P. Maszara, J. Electrochem. Soc. **138**, 341 (1991).
[22] S. Bengtsson, J. Electron. Mater. **21**, 841 (1992).
[23] K. Mitani and U. Gösele, J. Electron. Mater. **21**, 669 (1992).
[24] Ch. Harendt, H.-G. Graf, B. Höfflinger, and E. Penteker, J. Micromech. Microeng. **2**, 113 (1992).
[25] Q.-Y. Tong and U. Gösele, Mater. Chem. Phys. **37**, 101 (1994).
[26] F. S. d'Aragano and Lj. Ristic, in *Sensor Technology and Devices*, edited by L. Ristic (Artech House, Boston, 1994), Chap. 5, p. 157.
[27] Y. H. Lo, Z. H. Zhu, Y. Qian, F. E. Ejeckham, and G. L. Christenson, Proc. SPIE **3006**, 26 (1997).
[28] Y. Okuno, K. Uomi, M. Aoki, and T. Tsuchiya, IEEE J. Quantum Electron. **33**, 956 (1997).
[29] U. Gösele and Q.-Y. Tong, Annu. Rev. Mater. Sci. **28**, 215 (1998).
[30] A. Plössl and G. Kräuter, Mat. Science Eng., R. (in press).
[31] Special Issue on Direct Bonding, Philips J. Res. **49**, 1 (1995).
[32] Q.-Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology* (VCH–Wiley, New York) (in press).
[33] R. Stengl, K.-Y. Ahn, and U. Gösele, Jpn. J. Appl. Phys., Part 2 **27**, L2364 (1988).
[34] U. Gösele *et al.*, Appl. Phys. Lett. **67**, 863 (1995).
[35] S. Bengtsson, K. Ljungberg, and J. Vedde, Appl. Phys. Lett. **69**, 3381 (1996).
[36] W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, J. Appl. Phys. **64**, 4943 (1988).
[37] K. Ljungberg, A. Söderbärg, and Y. Bäcklund, Appl. Phys. Lett. **62**, 1363 (1993).
[38] Q.-Y. Tong, E. Schmidt, U. Gösele, and M. Reiche, Appl. Phys. Lett. **64**, 625 (1994).
[39] C. Gui, M. Elwenspoek, J. G. E. Gardiniers, and P. V. Lambeck, J. Electrochem. Soc. **145**, 2198 (1998).
[40] H. H. Yu and Z. Suo, J. Mech. Phys. Solids **46**, 829 (1998).
[41] Q.-Y. Tong and U. Gösele, J. Electrochem. Soc. **142**, 3975 (1995).
[42] U. Gösele, H. Stenzel, T. Martini, J. Steinkirchner, D. Conrad, and K. Scheerschmidt, Appl. Phys. Lett. **67**, 3614 (1995).
[43] K. Scheerschmidt, D. Conrad, A. Belov, and U. Gösele, Comput. Mater. Sci. **6**, 108 (1997).
[44] A. Plössl, R. Scholz, J. Bagdahn, H. Stenzl, K. N. Tu, and U. Gösele, Proc. Electrochem. Soc. **97–36**, 1361 (1998).
[45] T. R. Chung, N. Hosoda, T. Suga, and H. Takagi, Appl. Phys. Lett. **72**, 1565 (1998).
[46] K. Ljungberg, F. Grey, and S. Bengtsson, Appl. Surf. Sci. **117–118**, 813 (1997).
[47] K. Hobart, M. E. Twigg, F. Kub, and C. A. Desmond, Appl. Phys. Lett. **72**, 1095 (1998).
[48] M. K. Weldon, Y. J. Chabal, D. R. Hamann, S. B. Christman, E. E. Chaban, and L. C. Feldman, J. Vac. Sci. Technol. B **14**, 3095 (1996).
[49] Y. J. Chabal *et al.*, J. Vac. Sci. Technol. A **13**, 1719 (1995).
[50] M. K. Weldon *et al.*, Surf. Sci. **368**, 163 (1996); M. K. Weldon *et al.*, Proc. Electrochem. Soc. **97–36**, 229 (1997).
[51] S. Mack, H. Baumann, and U. Gösele, Sens. Actuators A **56**, 273 (1996).
[52] S. Mack, H. Baumann, U. Gösele, H. Werner, and R. Schlögl, J. Electrochem. Soc. **144**, 1106 (1997).
[53] G. Kräuter, A. Schumacher, and U. Gösele, Sens. Actuators A **70**, 271 (1998).
[54] T. Abe, M. Nakano, and T. Itoh, in *Proceedings of the 4th International Symposium Silicon-on Insulator Technologies and Devices* [Proc. Electrochem. Soc. **90–6**, 61 (1990)].

[55]Q.-Y. Tong, W. J. Kim, T.-H. Lee, and U. Gösele, Electrochem. and Solid-State Lett. **1**, 52 (1998).

[56]O. Zucker, W. Langheinrich, and M. Kulozik, Sens. Actuators A **36**, 227 (1993).

[57]S. Farrens, J. R. Dekker, J. K. Smith, and B. F. Roberds, J. Electrochem. Soc. **142**, 3949 (1995).

[58]M. Reiche, K. Gutjahr, D. Stolze, D. Burczyk, and M. Petzold, in Ref. 18, p. 437.

[59]P. Kopperschmidt, S. Senz, G. Kästner, D. Hesse, and U. M. Gösele, Appl. Phys. Lett. **72**, 3181 (1998).

[60]P. Kopperschmidt, G. Kästner, D. Hesse, and U. Gösele, Appl. Phys. A: Mater. Sci. Process. **64**, 533 (1997).

[61]P. Kopperschmidt, St. Senz, R. Scholz, and U. Gösele, Appl. Phys. Lett. **74**, 374 (1999).

[62]St. Senz (personal communication).

[63]M. Bruel, Electron. Lett. **31**, 1201 (1995).

[64]M. Bruel, B. Aspar, and A. J. Auberton-Herve, Jpn. J. Appl. Phys., Part 1 **36**, 1636 (1997).

[65]Q.-Y. Tong, R. Scholz, U. Gösele, T.-H. Lee, L.-J. Huang, Y.-L. Chao, and T. Y. Tan, Appl. Phys. Lett. **72**, 49 (1998).

[66]Q.-Y. Tong, L.-J. Huang, Y.-L. Chao, A. Ploessl, and U. Gösele, Proceedings of the 1998 IEEE SOI Conference, Florida, Oct. 1998, p. 143.

[67]M. K. Weldon *et al.*, Appl. Phys. Lett. **73**, 3721 (1998).

[68]C. Ascheron, A. Schindler, R. Flagmeyer, and G. Otto, Nucl. Instrum. Methods Phys. Res. B **36**, 163 (1989), and references therein.

[69]L.-J. Huang, Q.-Y. Tong, Y.-L. Chao, T.-H. Lee, T. Martini, and U. Gösele, Appl. Phys. Lett. (submitted).

[70]L. Di Cioccio, Y. Le Tiec, F. Letertre, C. Jaussaud, and M. Bruel, Electron. Lett. **32**, 1144 (1996).

[71]Q.-Y. Tong, K. Gutjarh, S. Hopfe, U. Gösele, and T.-H. Lee, Appl. Phys. Lett. **70**, 1390 (1997).

[72]E. Jalaguier, B. Aspar, S. Pocas, J. F. Michaud, M. Zussy, A. M. Papon, and M. Bruel, Electron. Lett. **34**, 408 (1998).

[73]Q.-Y. Tong, L.-J. Huang, Y.-L. Chao, R. Scholz, and U. Gösele, Appl. Phys. Lett. (submitted).

[74]J. Woltersdorf and E. Pippel, Thin Solid Films **116**, 77 (1984).

[75]L. B. Freund and W. D. Nix, Appl. Phys. Lett. **69**, 173 (1996).

[76]D. Teng and Y. H. Lo, Appl. Phys. Lett. **62**, 43 (1993).

[77]F. E. Ejeckham, Y. H. Lo, S. Subramanian, H. Q. Hou, and B. E. Hammons, Appl. Phys. Lett. **70**, 1685 (1997).

[78]F. E. Ejeckham, M. L. Seaford, Y. H. Lo, H. Q. Hou, and B. E. Hammons, Appl. Phys. Lett. **71**, 776 (1997).

[79]Z. H. Zhu, R. Zhou, F. E. Ejeckham, Z. Zhang, J. Greenberg, Y. H. Lo, H. Q. Hou, and B. E. Hammons, Appl. Phys. Lett. **72**, 2598 (1998).

[80]Z. L. Liau and D. E. Mull, Appl. Phys. Lett. **56**, 737 (1990).

[81]Z.-H. Zhu, F. E. Ejeckham, Y. Qian, J. Zhang, Z. Zhang, G. L. Christenson, and Y. H. Lo, IEEE J. Sel. Top. Quantum Electron. **3**, 927 (1997).

[82]Y. H. Lo and Z. H. Zhu, Technical Digest 1998 International Conference Solid State Dev. Materials (1998), p. 228.

[83]A. S. Brown, J. Vac. Sci. Technol. B **16**, 2308 (1998).

[84]G. Kästner, U. Gösele, and T. Y. Tan, Appl. Phys. A: Mater. Sci. Process. **66**, 13 (1998).