Annu. Rev. Mater. Sci. 1998. 28:79–100

HIGH-DIELECTRIC CONSTANT THIN FILMS FOR DYNAMIC RANDOM ACCESS MEMORIES (DRAM)

J. F. Scott
Max-Planck Institute for Microstructural Physics, Halle, Saale D-06120, Germany;
School of Physics, University of New South Wales, Sydney 2052, NSW, Australia

KEY WORDS: ferroelectric, oxide ferroelectrics, perovskite structures, capacitors

ABSTRACT

We discuss high-dielectric films, in general, oxide ferroelectrics based on simple perovskite structures and related Aurivillius-phase layered structure perovskites employed as thin-film capacitors in dynamic random access memories (DRAMs). Emphasis is on breakdown mechanisms and limits, leakage currents, electrodes and electrode interfaces, scaling to submicron geometries, and deposition techniques.

INTRODUCTION AND EXISTING TECHNOLOGY

The capacitors in random access memories (RAMs) have traditionally been fabricated by controlled oxidation of the free surfaces of the silicon integrated circuit. This produces a robust, chemically stable reliable thin-film capacitor, but with the disadvantage that the dielectric constant is small ($\sim$6). In order to obtain the required charge storage density of $\sim$30 f F/cell for a 64 Mb RAM (1), it has been necessary to fabricate complicated geometries with stacking and trenching, simply to add surface area requisite to achieve the desired total capacitance per cell. If a material with 100 times the dielectric constant could be employed, then the required surface area would be 100 times smaller, and stacking and trenching could be eliminated for the present generation of RAMs (up to 64 Mb), permitting reversion to a planar technology with fewer processing

0084-6600/98/0801-0079$08.00

steps and higher yields; or alternatively, the new material could be combined with stacking and trenching to make possible multi-Gbit memories, for which the existing stack/trench technology is rapidly reaching practical limits at 0.1 micron length scales.

Conventional dynamic RAMs (DRAMs) now employ either SiO_2 capacitors, as discussed above, or a combination of SiO_2 and Si_3N_4 nitride, which is termed ONO (oxy-nitride).

The next generation of RAMs was intended to utilize Ta_2O_5 to replace ONO, but the tantalum oxide dielectric constant is only about 25, and it appears that the RAM evolution will skip this intermediate stage and pass directly to very high dielectric materials ($\varepsilon = 500$–1500) that are ferroelectric or nearly ferroelectric. Many of these materials are oxides of the ABO_3 perovskite family, or closely related variations of perovskites. A good review of this technology is given by Gnade et al (2) (see also Kotecki 2a).

In going from 64 Mb to 4 Gb, the area per cell decreases such that the capacitance per unit area must increase from 30 to 140 f F/μm^2; concomitant with this increase is a decrease in operating voltage from 3.3 to 1.1 V that will necessitate a decrease in film thickness by a factor of 3 in order to maintain operation at constant electric field levels (2). Thus primary interest lies in the consideration of the feasibility and effects of areal and thickness reductions.

Reviews by Tasch & Parker (3) and Mochizuki (4) focused attention on the prospect of using high-dielectric (ferroelectric) films for DRAM capacitors. A related review on nonvolatile RAMs also focused on the general use of ferroelectric thin films in RAMs (5).

At this stage of development (1991), the processing problems of integrating high dielectric perovskite oxides as thin-film capacitors into microelectronic devices had already been solved. The use of barium strontium titanate (BST) capacitors in GaAs MMICs for 2.3 GHz operation had been accomplished by a Symetrix-Matsushita collaboration, resulting in the commercial production in 1992 of five different barium strontium titanate ($Ba_xSr_{1-x}TiO_3$ with $x \sim 0.7$ for maximum dielectric constant at ambient temperatures) GaAs chips at Panasonic-National: GN2012, a mixer IC with a 500 pF BST bypass capacitor; GN1016, a wide-band amplifier with high (12 dB) gain and low (2.6 dB) noise; GN1025, a low-noise amplifier with slightly higher gain (15 dB); GN2014, an integrated mixer with local amplifier and low distortion (12 dBm); and GN1023, a one-chip front-end IC with 22 dB gain. In 1994 these products won the Nikkei Shimbun award as "Product of the Year" in the Japanese electronics industry. By 1996 their production had reached 300,000 chips/month, and 5 million chips/month in 1997, primarily for digital mobile telephones but also for TV. In 1992, the same 500 pF BST capacitor was also successfully integrated into a Si 8-bit microprocessor by Symetrix-Matsushita, so that BST was

not viewed as an untested substance when subsequently introduced as a capacitor in DRAMs. The commercial experience and familiarity with BST/Si and BST/GaAs in these years should not be underestimated in reviewing the history of ferroelectric thin-film DRAMs, especially those using BST. Very detailed studies of failure in such films are under recent study; see especially the Weibull plots of Noma & Ueda (6), who found that larger grain sizes minimize aging. These devices were first reviewed by Mochizuki (7), with explicit connection to the utilization of the same materials for DRAMs [for recent review see (8)].

MATERIALS

In these relatively early years considerable work was also carried out at NEC, primarily on pure strontium titanate (no barium) but also on BST, generally prepared as sputtered films (9).

BST can be processed by physical deposition, especially sputtering, with good results (10); MOCVD also works well (11). The best performance parameters given thus far for strontium titanate are by No (12), who reported a dielectric constant greater than 300, very low loss ($\tan\delta \sim 0.01$), and breakdown fields exceeding 300 MV/m; those for BST are from Hwang et al (13), with dielectric constant a modest 325, but a storage capacitance of 145 f F/μm^2 was achieved via very thin films (20 nm). The best value of dielectric constant reported for BST thin films is from McMillan, using liquid source deposition (14).

Other good results for BST DRAM films were reported by Kawahara et al (15), Takemura et al (16), Hwang et al (13, 17), and Yoshida et al (18). Recently a United States consortium has duplicated many of the earlier results from Japan and Korea (19). Prototype BST-capacitor DRAMs have also been reported by Yamauchi et al (20), Nishioka et al (21), and Lee et al (22).

The second material to receive great attention for use as a DRAM capacitor (and also for nonvolatile RAMs) is PZT (lead zirconate titanate: $PbZr_{1-x}Ti_xO_3$, with $0.4 < x < 0.6$). This material is not discussed at any length in this review because it is the author's contention that it is not a viable candidate for DRAM applications. Although its dielectric constant is large ($\sim$1300) even in thin-film form, its leakage current is too high; it cannot be consistently and reliably prepared in the very thin thicknesses required for DRAMs with maintainence of good dielectric parameters due to surface layers at the electrode interface; Pb volatility is a problem; and, in general, PZT is not competitive with BST for DRAMs. We do note, however, that a few authors still refer to their work on PZT and/or lead lanthanum titanate (PLT) as generally suitable for DRAM or FeRAM (nonvolatile RAM) cells (23).

The third material of current interest is the $SrBi_2Ta_2O_9$ (SBT) family of layer-structure, A'urivillius-phase perovskites. Although initially studied for

nonvolatile RAMs, their properties are also suitable for DRAMs. SBT has a breakdown field of 280 MV/m (24) compared with 380 MV/m in BST, and its leakage current of 1.0 nA/cm^2 at 3.0 V across 100 nm (25) is equal to the best value ever reported for BST (26) and about 100 times better than typical BST values (11, 27, 28).

The only drawback of SBT has been its high processing temperatures ($>700^\circ$C), but a recent Mitsubishi-Sharp collaboration has produced excellent films at 600°C (29).

DEPOSITION

Sputtering

Sputtering of strontium titanate and BST films was carried out extensively by the NEC group, with recent extensions to SBT as well (30). Fundamental work on the electrochemistry of these materials had also been done by Waser et al (31–34). Lee et al (35) and Paek et al (36) recently reported rf magnetron sputtering of SBT.

Chemical Vapor Deposition (CVD)

CVD of BST was reported by Eguchi & Kiyotoshi (37), using Ba-, Sr-, and TiO-$(THD)_2$, where THD is 2,2,6,6-tetramethyl-3,5-heptadione. Conformal step coverage was obtained. A 773 K anneal was employed.

Metal-Organic Deposition (MOD)

MOD is the preferred deposition technique for BST. Recent studies include those by Noma & Ueda (6) and Joshi et al (38, 38a).

Metal-Organic Chemical Vapor Deposition (MOCVD)

BST and pure strontium titanate films of good quality have been prepared by MOCVD, by using titanium isopropoxide and $Sr(DPM)_2$ (39). Plasma enhanced MOCVD was reported using Ti isopropoxide and $Sr(hfa)_2$(tet) (hexafluoroacetyl-acetonate-tetraglyme: "ack-ack") (40–42) and in Eu-doped systems (43).

Liquid Source Mist Deposition (LSCVD)

In the liquid source deposition process, stoichiometrically correct precursor mixes are injected into a deposition chamber through a nozzle to produce very fine (0.1–1.0 micron diameter) droplets. This mist technique was developed by McMillan et al (14). It works exceptionally well for PZT, SBT, and BST. A recent status report emphasizing conformal coverage obtained is given by Solayappan et al (44).

Other liquid source CVD studies of BST deposition (44a) involve dissolving precursors such as bis(dipivaloylmethanato) barium and strontium into

tetrahydrofuran and using a variety of titanium precursors such as bis(isopropoxy) bis(dipivaloylmethanato) titantium, titanyl bis(dipivaloylmethanato), or titanium tetraisopropoxide.

A peripherally related aerosol technique for BST deposition was reported by Kussmaul et al (45).

Flash CVD

To overcome the low viscosity of precursors used for SBT deposition, Isobe et al developed a system in which liquid precursors are delivered to the deposition chamber and then flashed to a vapor state immediately before deposition. High throughput is achieved in this system (46); deposition rates are about 50% of those with mist deposition (14).

Pulsed Laser Deposition (PLD)

Some recent texts have been largely devoted to PLD, particularly of ferroelectrics (47–49). Singh et al (49) give a good comparison between sol-gel and PLD SBT films, including comparisons for Pt, oxide, and hybrid (49) electrodes; and Chrisey et al (49) examine optoelectronic applications.

Pulsed laser deposition of BST has most recently been reported by Jia et al (50). They used the RuO_2 electroding preferred by NEC (RuO_2 top and bottom electrodes, compared with the elemental Ru utilized by Mitsubishi, or the Pt used by Samsung and the United States DRAM consortium).

Laser ablation of pure strontium titanate has also been reported by Miranda et al on high-T_c superconducting electrodes (51). PLD of SBT has been carried out with good results by Thomas et al (52), Yang et al (53), and Tabata et al (54), with Pignolet et al (55) achieving the largest area (20 cm^2) of uniform coverage (see also 56). PLD of bismuth titanate has been reported by Park et al (57), Watanabe et al (58), and Choopun et al (59).

Solution-Gelation

Sol-gel spin-on is still used for SBT. Recent studies include the Sandia report (60), in which Sr- and Bi-acetate and tantalum ethoxide precursors were used, and related work on sol-gel BST (61), including Sr dependence (62). Two reviews of sol-gel ferroelectrics are given by Xu et al (63, 64)

SCALING TO SUBMICRON SIZES

Area

The main limitation on lateral area of DRAM cells is due to fringing fields. Calculation of the total charge switched for a capacitor as a function of aspect ratio (diameter to thickness) is a standard problem in electrostatics. For large

aspect ratios, the correction is small: A 10:1 aspect ratio involves ~7% correction depending on shape (circular, rectangular, square), and the 5:1 aspect ratio most recently employed at NEC (square capacitors 0.7 microns on a side by 0.2 microns thick) involves roughly a 20% correction. For aspect ratios closer to unity, as may occur in submicron Gbit DRAMs, the correction term diverges (implying that the lines of force are not perpendicular to the capacitor top and bottom surfaces, but perhaps terminate on DRAM sidewalls). In this case, it is better to solve Laplace's equation for a box or cylinder shape corresponding to the actual capacitor geometry. Unfortunately, although this approach yields accurate field contours and isopotential surfaces, it is useless for calculating the time dependence of the DRAM response (charging or discharging), because Laplace's equation is not generally valid in the time-varying case. Here it is necessary to go back to numerical solutions of Maxwell's equations. However, the qualitative features of scaling can be seen by calculating the capacitance of a rectangle of width a and length b, such that $d \ll a \ll b$, where d is the film thickness. This leads to the result that switched charge Q is not proportional to the surface area ab, but rather to $b \log a$. This $\log a$ dependence agrees with the experimental results of Amanuma & Kunio (65) on $0.7 \times 0.7 \times 0.2$ micron SBT films.

Of equal importance is the dependence of the breakdown field upon capacitor surface area. If we assume, using the basic model of Gerson & Marshall (66) [see also Duiker et al (67, 68)], that breakdown is due to shorting along a linked path of defects or voids that have a particular threshold, then the odds of finding one such short as a function of capacitor area can be calculated directly.

First we note that Ohm's law is satisfied in insulators or semiconductors only where $aeE \ll kT$, where a is a lattice constant; e, the electron charge; E, the applied field; k, Boltzmann's constant; and T, temperature. For perovskite oxides at 250 kV/cm, this condition breaks down, and exponential conduction results. This implies that current density

$$J = q/t = D \exp(cE). \qquad 1.$$

The breakdown time t_B and breakdown field E_B are related by

$$q/t_B = D \exp(cE_B). \qquad 2.$$

The latter equation can be rewritten as

$$\log t_B = B - gE. \qquad 3.$$

That is, the log of the breakdown time is proportional to applied field.

Figure 1 shows that this equation is satisfied in BST up to ~100 MV/m. Figure 2 shows that at a higher field of 140 MV/m, there is a large variance in

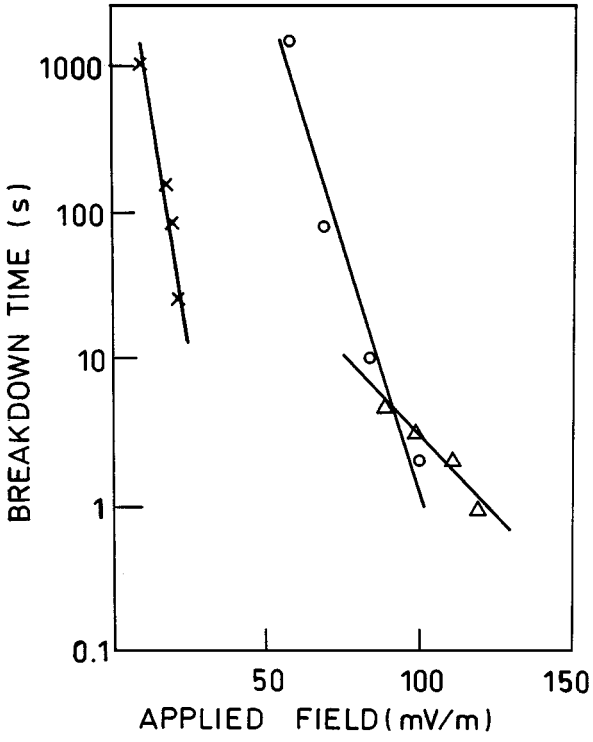

Figure 1 Breakdown time versus applied field in BST (*triangles*), pure strontium titanate (*circles*), and PZT (*crosses*) (56).

the breakdown times (although, the breakdown field is approximately constant for short measuring times). This large variance is a signature of avalanche mechanisms that are electronically initiated but reach fruition because of thermal runaway.

The areal dependence of the breakdown field follows the assumption that there is a Maxwell-Boltzmann distribution of defect energies that can produce microshorts:

$$n(E) = n_o \exp[bE/kT]. \quad 4.$$

Here b is a temperature-independent parameter with dimensions of an effective charge.

Assuming an axially isotropic distribution of such short-producing pathways from the center of the electrode,

$$n(r) = r^2 n(E). \quad 5.$$

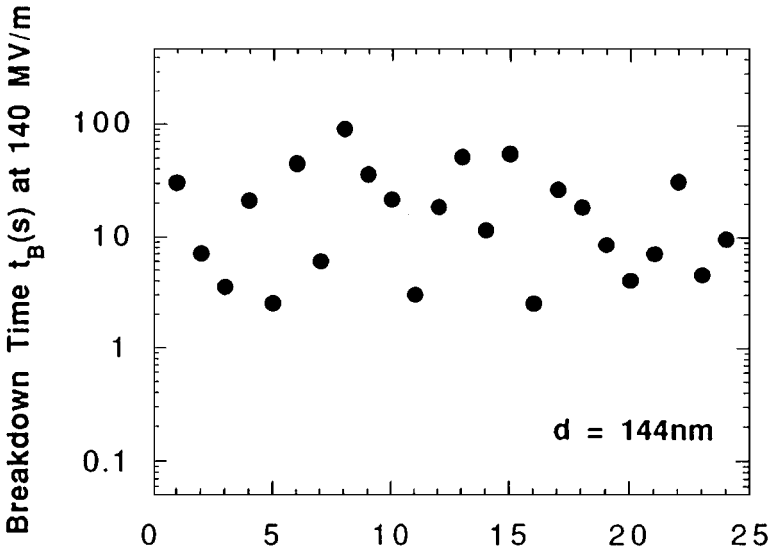

Figure 2 Variance in breakdown times at constant field for BST (56).

One finds that the probability of producing one short at a field E and temperature T is

$$1 = n_o r^2 \exp[bE_B/kT], \tag{6.}$$

from which

$$bE_B/kT = -\log n_o - \log A + \log \pi. \tag{7.}$$

where A is the electrode area πr^2.

Hence

$$E_B = h(T) - (kT/b) \log A, \tag{8.}$$

the breakdown field will decrease linearly with increasing T [shown experimentally in Figure 3 (69, 69a,b)] and decrease logarithmically with capacitor area A (Figure 4) (24).

Duiker et al extended this model of breakdown to a specific microscopic numerical algorithm: They assumed initial nucleation of an oxygen-depleted dendrite-like conducting path in the ferroelectric (Figure 5), which grew with successive voltage pulses. Each dendritic tree could add an ion (or oxygen vacancy) with time or lose one. But if the additional ion (or oxygen vacancy) touched two adjacent ion/vacancies, it became irreversibly pinned. The evolution of these dendritic microshorts is shown in Figure 5. Raleigh argued earlier

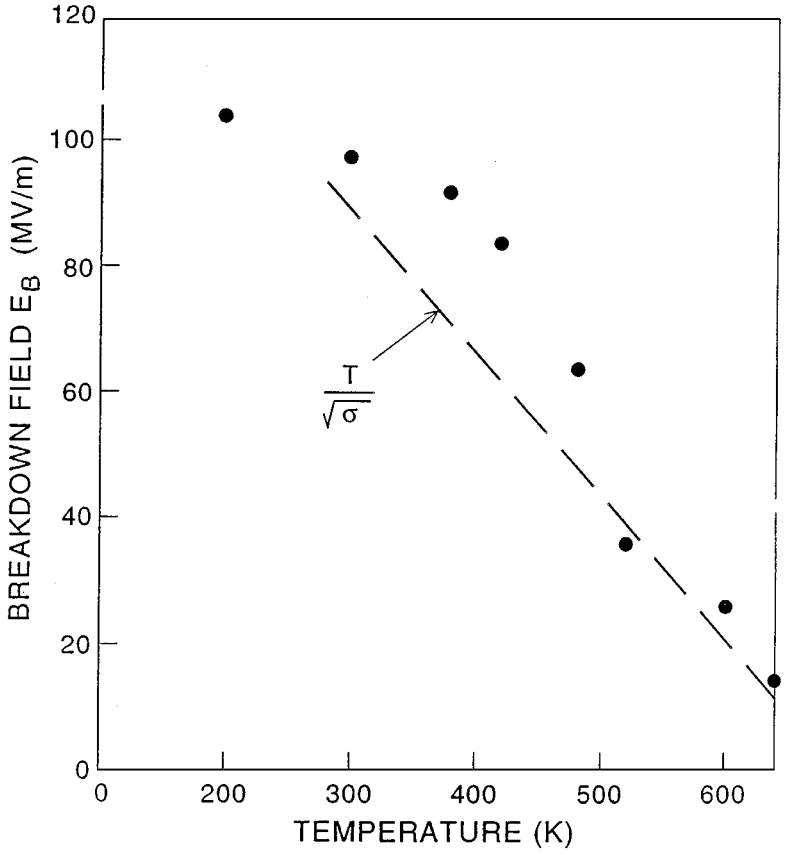

Figure 3 Breakdown field versus temperature for PZT. Results for BST are similar (56).

(70) that such growth was favored at interfaces that were atomically rough or on conducting oxide electrodes even if atomically smooth. Recently, DeVeirman et al (71) found such shorts in PZT on oxide electrodes but not in PZT on Pt electrodes, confirming Raleigh's prediction.

Thickness Dependences

The thickness of a ferroelectric DRAM is of greatest concern in its effect on leakage current and on breakdown. For a DRAM, the maximum acceptable leakage current is about 10 μA/cm^2, for the desired operating voltage (1.1–3.3 V) across a thickness of 100 nm or less. For PZT this is unattainable; for BST it is difficult but not impossible; for SBT it is easy.

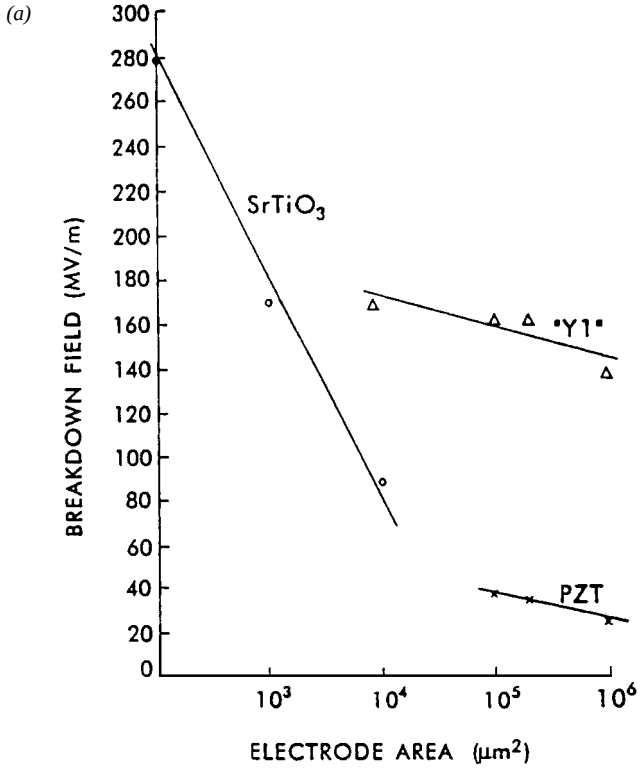

Figure 4 (*a*) Breakdown field versus capacitor area for strontium titanate, PZT, and SBT ("Y1").

The breakdown field obtainable with BST is about 150 MV/m. For a comfortable safety margain in a 4 Gb DRAM with 1.1 V operating levels, this means that even 30 nm thickness could be used.

The fact that leakage current is relatively independent of thickness for most BST films and that it displays a polarity dependence (Figure 6) (72) indicates that it is not Poole-Frenkel conduction. Poole-Frenkel is a bulk process; it is polarity independent and strongly dependent upon thickness. Most authors agree with this point of view; however, Hwang et al (73) argue that leakage current in BST is primarily Poole-Frenkel and not Schottky.

Above 300–400 kV/cm in BST, Fowler-Nordheim tunneling becomes dominant, as first established by Scott et al (74) (see Figure 7) and later confirmed by Waser (75).

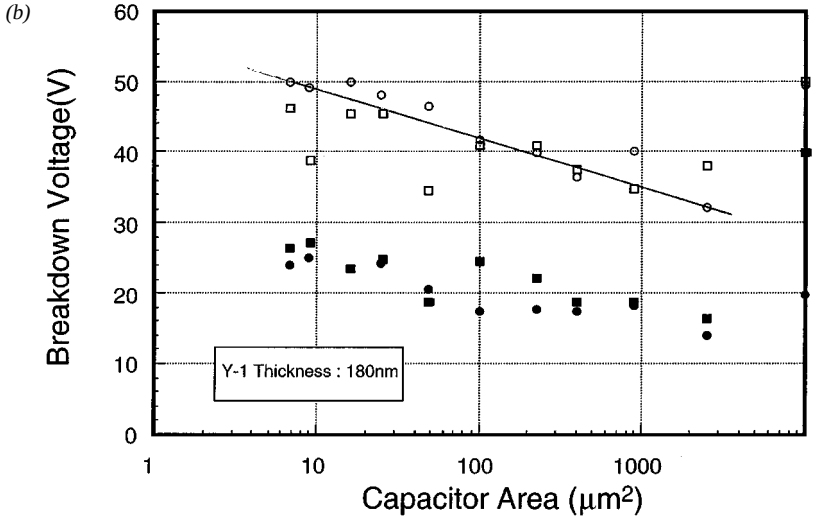

Figure 4 (*b*) More detail for improved SBT (24), with 50 V across 180 nm at 10 μm^2 (278 MV/m).

ELECTRODES

Elemental Metal Electrodes

In SBT/Pt the band models of the Pt interface are not compatible with an abrupt Schottky model. The Pt work function Φ is 5.3 eV. The measured Schottky barrier height is 0.9 eV (76, 77). But the SBT electron affinity χ is 3.4 eV (XPS data; 78).

The Schottky barrier height should be $\Phi - \chi$ for an abrupt Schottky barrier. Therefore, 1.0 eV needs to be accounted for via either a graded junction or an insulating defect layer between the Pt and the SBT. For PZT, with a large 20 nm damage layer at the electrode interface, the problem is more severe.

To understand the role of electrodes in DRAMs, it is helpful to begin with a band model of the ferroelectric-electrode interface (79). The correct model of PZT or BST on Pt (80) is that of a p-type wide-bandgap semiconductor with an n-type inversion layer at the Pt interface. It is important that the Pt work function of 5.3 eV is greater than the ferroelectric bandgap of ~3.6–4.0 eV.

More detailed measurements and calculations have been made recently for SBT/Pt (Figure 8). Calculation of the Schottky barrier height in SBT on Pt is an interesting problem. Although the index $S = d\Phi_{Bn}/dX$ (where X is the electronegativity of the ferroelectric) of interface behavior for such an ionic ABO_3 perovskite is nearly unity (81), the very large density of surface states

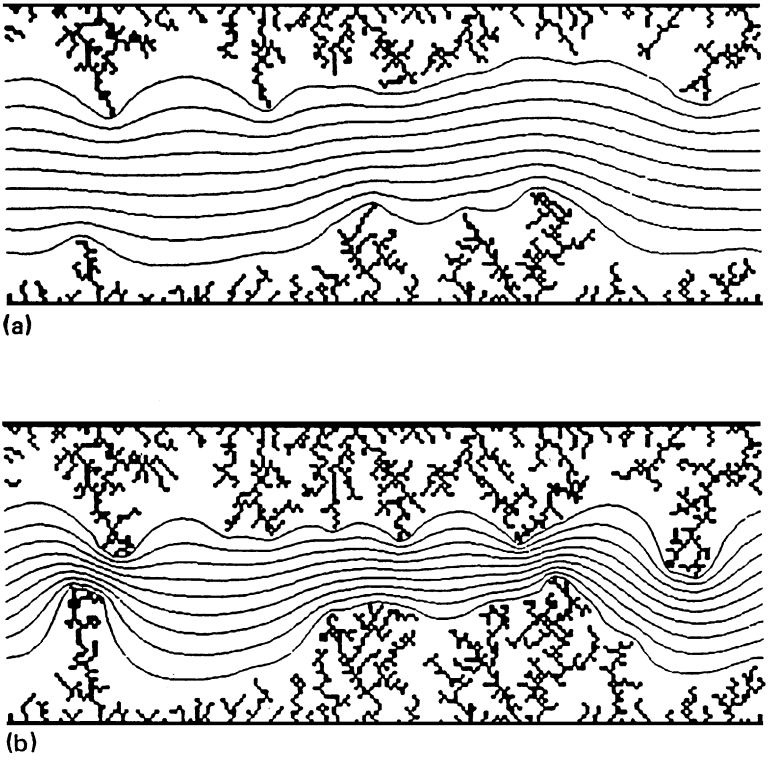

Figure 5 Dendritic short model (67, 68).

compensates for the ionicity, resulting in an interface condition that is midway between the covalent, trap-limited case and the more ionic, trap-free situation, often considered a limiting case (82).

The Schottky barrier height is given approximately (83) by

$$\Phi_{Bn} = [c(\Phi M - \chi) + (1 - c)(Eg - \Phi_o) - \Delta\Phi]. \quad 9.$$

Here

$$c = 2q\varepsilon N\delta^2/\varepsilon_i^2, \quad 10.$$

where q is the electron charge; ε, the dielectric constant of SBT ($\sim$500); N, the density of acceptors; δ, the width of the interfacial layer between the Pt and the SBT; and ε_i, the dielectric constant of that layer. One can see in Equation 10

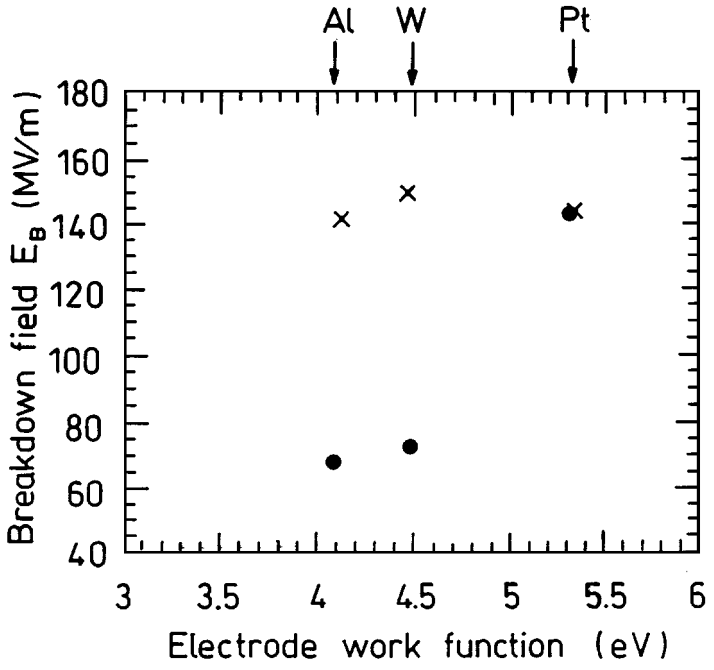

Figure 6 Polarity dependence of breakdown field in BST (56).

that a large trap density N can be compensated for linearly by a large interfacial dielectric constant ε_i, provided that ε_i is comparable to the dielectric constant, ε, of the ferroelectric semiconductor itself.

With an estimate of 5×10^{14} surface traps per cm^2 (84–86), we can approximate $c = 0.7$ for SBT/Pt (87). The numerical value of the barrier height is not very sensitive to this value; $c = 1.0$ for purely ionic models with no surface-state Fermi level pinning, and $c = 0$ for a purely covalent semiconductor with very high surface trap density ($c = 0.27$ in Si). Hence c in SBT must be much greater than 0.27 and less than 1.0.

For Pt $\Phi M = 5.3$ eV; we measure $\chi = 3.4$ eV for SBT via XPS; Eg = 4.2 eV from UV absorption; Φ_o is the energy level at the surface (the SBT Fermi level versus the SBT valence band level), which from our XPS data is 2.1 eV—approximately half the bandgap. By comparison, the values of Φ_o in Si, GaP, or GaAs are always around 0.3 Eg, increasing to ~0.6 Eg in more ionic II-VI compounds such as CdS (88), so this result is reasonable.

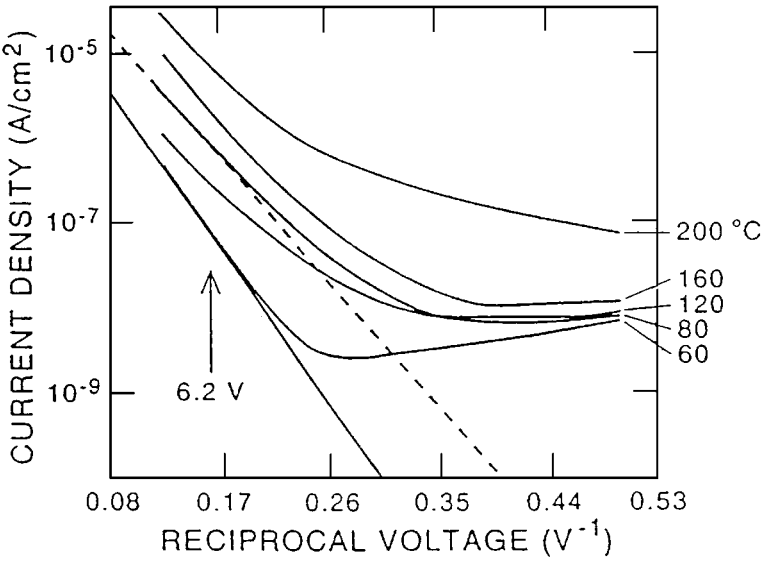

Figure 7 Leakage current in BST versus applied field, showing Schottky behavior below and Fowler-Nordheim tunneling above 300 kV/cm (55).

This gives

$$\Phi_{\mathrm{Bn}} = 0.7 \times 1.9\,\mathrm{eV} + 0.3 \times 2.1\,\mathrm{eV} - \Delta\Phi = 1.96 - \Delta\Phi. \qquad 11.$$

The image field barrier reduction energy is $\Delta\Phi$. It is given by $[\mathrm{qE}/(4\pi\varepsilon_{\mathrm{op}})]^{1/2}$, where ε is not the dc dielectric constant [because the electrons move through the interface in a time $t = (6\text{ nm})/(10^5\text{ m/s}) = 10^{-13}$ s much faster than the dielectric relaxation time, so that the ions are not perturbed, and the response is purely electronic] but approximately $n^2 = \varepsilon_{\mathrm{op}}$, where n is the index of refraction in the visible region, ~2.4. For this value of ε the Schottky barrier width is ~2 nm.

At the measuring voltages of ~2.0 V, $\Delta\Phi = 0.8 \pm 0.3$ eV [for comparison (88), it is 0.55 ± 0.22 eV in Si at the same field levels, the value being lower by the square root of the ratio of $\varepsilon_{\mathrm{op}}$, which is 11.7 in Si and $2.4 \times 2.4 = 5.8$ in SBT] and hence the SBT/Pt barrier height is calculated as 1.1 ± 0.3 eV.

Watanabe (76) measures 0.83 eV Schottky barrier height, and Lee et al (77) report 0.9–1.1 eV, which is in complete agreement with this calculation. Similar values are obtained by a careful fit of the Schottky emission in BST on Pt. In this case, Joshi et al (38) showed that the zero-voltage Schottky barrier height is 1.5 eV (compared with our value of 1.96 eV in SBT above) and that the barrier reduction value is 0.8 eV at 3 V (across 150 nm), exactly as we

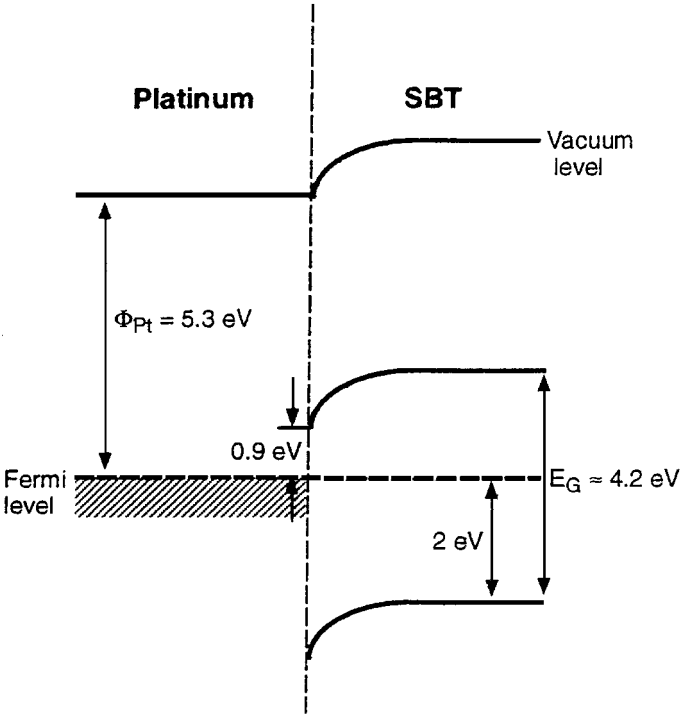

Figure 8 Interfacial band line-up model for SBT/Pt Schottky barrier (69); the structure is qualitatively the same in BST (62).

calculated for SBT, so that the reduced barrier height is 0.7 $\pm$ 0.2 eV for BST, in close agreement with our calculated value of 1.1 $\pm$ 0.3 eV for SBT and even closer to Watanabe's experimental value of 0.83 eV. Waser (38a) gives a slightly larger value of 1.1 eV for Ni-doped strontium titanate on Pt. Thus we see that band model calculations work well for these materials and that BST, PZT, and SBT films for DRAM capacitors all behave as wide-bandgap p-type semiconductors with n-type inversion layers at the Pt interface thermally populated at ambient temperatures. Under normal operating voltages of $\sim$3 V, they act as fully depleted devices so that all of the charge carriers are electrons injected from the cathode. This was first established by Melnick et al (89) and confirmed by Wouters et al (90).

Finally, we note that de Wette (91) has shown theoretically, via shell-model calculations, that for thin films of layer-structure bismuth-containing perovskite oxides (including high-T_c superconductors such as $Bi_2CaSr_2Cu_2O_8$) the surfaces

will terminate on Bi_2O_2 planes and not on ABO_3 cubes and that the Bi-O bond length relaxes (shrinks) by 0.011 nm for that layer. It is possible that this relaxed layer affects the Schottky barrier height significantly in SBT/Pt.

Metallic Oxide Electrodes

The use of metal oxide electrodes for ferroelectric thin-film DRAMs was pioneered by Ramesh and coworkers, as well as by Desu, Kingon, and others (92–105). The basic idea was to find an electrode material whose lattice match would permit epitaxial growth (or grain-oriented nearly epitaxial growth) of ABO_3 perovskite ferroelectric films, with consequent minimization of interfacial strain. Tuttle et al had shown that such strain was detrimental to device performance of ferroelectric thin films (106, 107). In addition, the oxide electrodes provide a source of oxygen ions, and it was already known that BST and PZT were oxygen depleted at the electrode interfaces (108–110).

Although the emphasis from Ramesh et al has been to utilize these ideas for nonvolatile RAMs, and in particular to minimize fatigue due to repetitive cycling, the importance may be equally great in minimizing charge injection in DRAMs. In this context it is useful to refer to earlier work by Robblee et al on charge injection from metal electrodes (111–116). She found that IrO_2 produced one order of magnitude improvement in the ability of electrode interfaces to withstand repetitive unipolar voltage pulses if iridium oxide (Ir can reversibly alter valence) was used instead of platinum. In this way the iridium/iridium oxide electrodes act as a buffer for injected charge and protect the dielectric from irreversible damage.

In addition to simple oxides such as IrO_2 and ruthenium oxide [the latter used as a top electrode on Sony nonvolatile RAMs because of its ability to withstand forming-gas anneals at 1000 K (117)], high-T_c superconductors are also used as DRAM and microwave capacitor electrodes (118–122). In this embodiment, the oxygen ions are thought to stabilize the ferroelectric interface. However, recently Watanabe & Sawamura (123) suggest that the fact that these high-temperature superconducting compounds are hole-conductors may be more important in this context than the presence of oxygen ions (recall that BST, PZT, and SBT are all p-type wide-bandgap semiconductors).

BOTTOM ELECTRODE BARRIER LAYER

SBT requires a processing temperature of $\sim 700^\circ$C. At such temperatures there are two problems: First, Pt top electrodes do not perform well in forming gas ambients. Katori et al (117) have shown that Ru-O top electrodes perform much better. Second is the more severe problem of Bi diffusion through the bottom electrode. If not solved, this would prevent the use of the 1T-1C (one-transistor, one-capacitor) memory cell design (124) for SBT memories. At the time of

this writing, the SBT bottom electrode materials problem has been solved, but the material is proprietary; Pd-Rh alloys may be involved (see 125).

PHYSICAL PROBLEMS

Blistering

When ferroelectrics such as BST are deposited on Pt/Ti/Si electroded substrates, blisters are often observed. This was first reported by McMillan et al (126) and by Kingon et al (127, 127a,b). The problem is eliminated by optimizing thermal processing, especially with rapid thermal annealing (RTA). A typical annealing cycle for BST is 60–90 s to a maximum of 810°C. This time is sufficiently short that the underlying Si circuitry is undamaged.

Hillocks

In addition to blisters, Pt hillocks arise (127, 127a,b) in BST/Pt/Ti/Si or related ferroelectric RAM structures. This is due to the diffusion of Ti through Pt (111) films, driven by the reaction of Ti + O from the oxide ferroelectric to form rutile and by the different thermal expansion coefficient of Pt and Si (which also causes broad delamination). It can be eliminated by annealing the Pt and making it thicker (∼300 nm).

Leakage Current Density

At leakage current densities much greater than 10 μA/cm^2, DRAM heating becomes a problem (128). Thus there is a trade-off between minimizing film thickness d to maximize capacitance and making dielectric film thickness greater to minimize leakage current. However, whereas the capacitance is linearly (and inversely) dependent upon thickness for good films in which surface layers are negligible, the leakage current varies nonlinearly (approximately exponentially) with $1/d$. One figure of merit for a good DRAM film is therefore given by capacitance per unit area divided by leakage current density. For SBT at 3 V logic levels this is approximately 130 f F/μm^2 divided by 1 nA/cm^2, which is 13,000 F/A = s/V. At 3 V that is a figure of merit of 39,000 s.

As shown in Figure 7 (73), the leakage current in BST is Schottky-dominated up to ∼300 kV/cm, above which Fowler-Nordheim tunneling becomes important or even dominant. The fact that Schottky mechanisms are more important than Poole-Frenkel is shown by the dependence on polarity, illustrated for BST in Figure 6 (74). Poole-Frenkel is a bulk mechanism and should be independent of polarity.

Breakdown

The breakdown in ferroelectric films for DRAMs is avalanche-like in the sense that it is electronically initiated by thermal runaway kinetics. It typically occurs

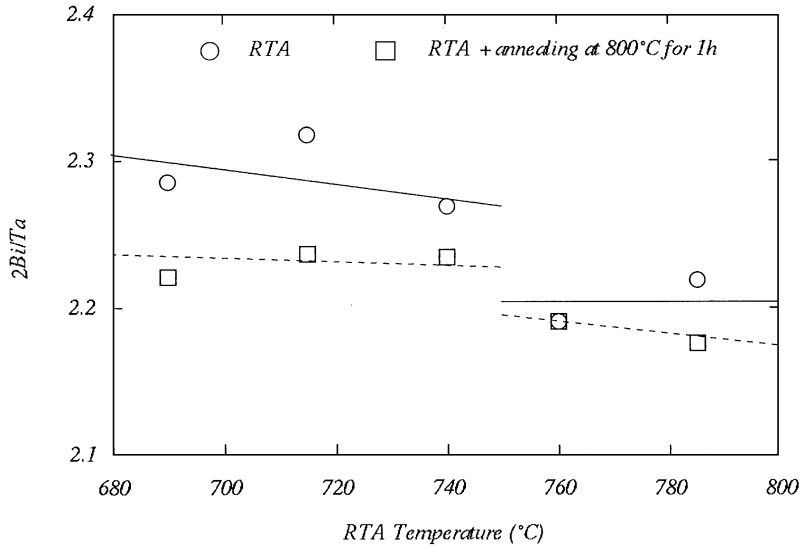

Figure 9 Bi-content ratio versus annealing temperature, showing a break at 750°C probably due to Bi-platinide production at the electrode interface (58).

at a specific current density threshold (not voltage or field threshold) so that its details depend on leakage current mechanisms (Figures 7, 9).

The primary parameter in determining the breakdown field is the contact potential between the metal electrode and the ferroelectric (usually a p-type wide-bandgap semiconductor). Figure 10 is a fit to the early theory of Von Hippel (129–131), which demonstrates this quite clearly. Here the slope is given by the electron mean free path in the ferroelectric (the data of Figure 10 give 0.1 nm at 295 K) and its intercept is simply related to the Schottky barrier height.

Sidewall Effects

The primary practical concerns about DRAM cell sidewalls are, first, that the lines of force may terminate on sidewalls, thus reducing the switched charge and net capacitance (a fringing field effect) and, second, that they may provide a route for hydrogen contamination of the ferroelectric/dielectric during forming gas anneal. In early ferroelectric RAM embodiments, such as the McDonnell-Douglas JFET device (junction field effect transistor), the ferroelectric edges could be exposed to silicon nitride or to polyimide. The edge configurations in the BST-stacked capacitor DRAM designs of NEC, Mitsubishi, or the United States DRAM consortium have BST between SiO_2 and a metal

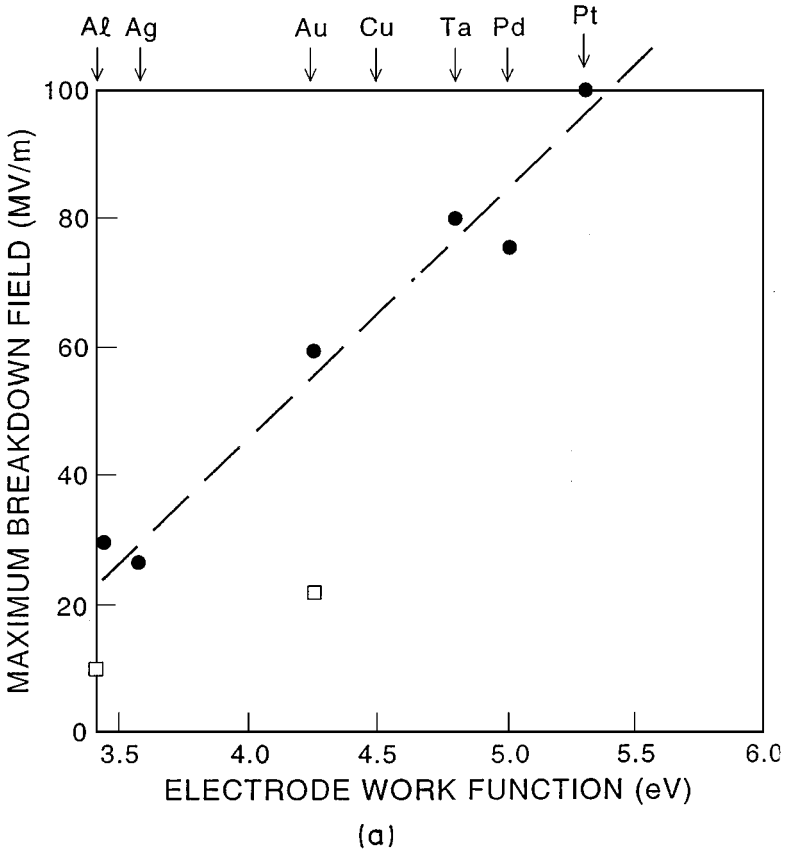

Figure 10 Breakdown field in BST versus electrode work function (56).

electrode (TiN/Al, Ru, or Pt, respectively). But the detailed sidewall geometries are somewhat proprietary. Care should be exercised in isolating the dielectric edges from any source of hydrogen diffusion.

DEVICE DESIGN

There are two different routes toward making a very high-density nonvolatile RAM. The first is to begin with low-density ferroelectric nonvolatile RAMs, perhaps using PZT and gradually scale up the bit density. The second route is to begin with a (volatile) DRAM of high density, probably employing BST and extend the refresh cycle time. These parallel development paths were first ennunciated by Kano in 1992 (132).

By employing SBT in DRAMs as well as nonvolatile FeRAMs, these parallel technology paths can use a single material. SBT has a dielectric constant of ∼500, which is better than that of most BST films. It has a high breakdown field (∼230 MV/m), and it can be prepared in thicknesses <100 nm without degradation of device parameters. Its leakage current of 1 nA/cm^2 at 3 V across 280 nm is very competitive.

Thus for long-refresh DRAMs, SBT is competitive with BST. For high-density FeRAMs, SBT's only drawback is its high processing temperature. However, recent developments include successful processing at 600°C, plus top (RuO) and bottom electrodes that, respectively, withstand forming gas anneal at 700°C and prevent Bi diffusion through the bottom electrode. At such temperatures, SBT and BST both appear to be viable ULSI DRAM materials. For nonvolatile devices, SBT has clear advantages over PZT.

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