Settling the “Dead Layer” Debate in Nanoscale Capacitors

By Li-Wu Chang, Marin Alexe, James F. Scott, and J. Marty Gregg

Whether interfacial “dead layers”, thought to be responsible for the orders of magnitude collapse in the polarizability of thin film capacitor structures, really exist or not has been a contentious issue for almost 50 years.[1] This has been despite the obvious importance that such dead layers have in limiting the successful utilization and integration of high permittivity materials into micro and nanoelectronics, and the large amount of literature that has been generated to date on the subject. Recently, though, significant steps towards understanding the nature of dead layers have been taken through both clean experiments on thin single crystal ferroelectrics[2,3] and state-of-the-art atomistic simulations modeling.[4] Unfortunately, until very recently, the implications of experiments and modeling appeared to conflict with each other: experiments concluded that dead layers could be engineered out of capacitor structures, while modeling concluded that dead layers were an unavoidable and inherent feature of the dielectric-metal interface. This year has seen a partial resolution of the scientific impasse with new models by Stengel, Vanderbilt, and Spaldin[5] suggesting that while dead layers are normally an unavoidable phenomenon, they are not present in the specific combination of ferroelectric and electrode materials that were chosen in the single crystal thin film experiments done to date.[2,3] Such a statement clearly ameliorates the conflicting points of view, but is incomplete without corresponding experiments on systems which had previously been modeled as showing unavoidable and inherent dead layer phenomena. This article closes the loop by presenting the results of just such an experimental study on thin single crystal SrTiO3 lamellae with platinum electrodes. These new measurements show that intrinsic dead layers are indeed present for this specific system while not in evidence for the analogous investigations on BaTiO3. Thus, now experiment and theory are in complete agreement — dielectric dead layers are an inherent feature of many dielectric-metal interfaces, but can be engineered out in specific cases where there is particularly weak interface bonding.

In theory, the performance of many electronic devices could be dramatically enhanced by incorporating ferroelectric materials into their structures. Ferroelectrics have a lot to offer: the reversible remanent polarization, which defines the ferroelectric, can be used for both non-volatile binary data storage and for altering local electric fields in field-effect transistors;[6,7] the high dielectric permittivities in these materials can be used for efficient dynamic charge storage in DRAM memory elements,[8] and the degree to which the permittivity can be altered using bias electric fields (the tunability) makes ferroelectrics extremely useful for smart tunable antennae,[9] as well as for photonic and plasmonic devices where field-controlled variations in refractive index are needed.[10–12] In practice, though, it is a frustrating irony that the key functional properties that make ferroelectric materials so attractive in the first place are almost universally observed to be degraded when in the form of a thin film, as is usually needed for the kinds of devices mentioned. In general, coercive fields increase,[13,14] tunability decreases and permittivities are severely suppressed, often by several orders of magnitude.[15]

Despite having been first observed around half a century ago,[1] the reason why the permittivity of ferroelectrics is so radically affected at reduced dimensions is still not understood. Most research points to the existence of a parasitic low permittivity layer, assumed to be associated with the ferroelectric-electrode boundary and often called the "dead layer". However, views on what physically constitutes a dead layer, and whether or not dead layers really even exist, are divided. There are some who claim that a low permittivity "interfacial capacitance" is intrinsic and unavoidable: an inevitable consequence of the physics of joining a material which sustains an internal polarization (the ferroelectric), to one which does not (the metal).[16–21] This view has been supported by established continuum physics as well as by recent atomistic simulations modeling.[5] Equally, there are those who claim that dead layers are entirely extrinsic in origin, and not fundamental at all, arising instead from imperfections in thin film processing or device design.[22–28] This view is supported by recent experiments performed on a 'model system' where processing deficiencies were minimized by cutting thin film lamellae directly from bulk single crystals of BaTiO3, using a focused ion beam, and annealing in oxygen to recrystallize any beam-induced damage.[29] Functional characterization of these kinds of thin film lamellae demonstrated no suppression in permittivity even in films as thin as ~75nm.[3]

How can these diametric views in scientific opinion be resolved? One significant step has been taken recently by Stengel, Vanderbilt, and Spaldin.[5] They have extended earlier atomistic simulations analysis to specifically include a consideration of the Au/BaTiO3/Au and Pt/BaTiO3/Pt thin film capacitor combinations that had been investigated experimentally by Saad et al.[3] and Chang et al.[2] respectively. Moreover, they have contrasted modeled behavior in these systems with others containing PbTiO3, perceived to be a "stronger" ferroelectric than BaTiO3,
with a significantly higher Curie temperature and larger spontaneous polarization. The conclusions of their work are both surprising and profound: firstly, the nature of the ferroelectric-electrode interfaces that develop act to destabilize ferroelectricity in Pt/TiO₂ to a much greater extent than in BaTiO₃; secondly, that while sources of inherent interfacial capacitance, or “dead layers” develop in the Pt/TiO₂ capacitors, no such dead layers develop in the specific combinations of elemental metals and BaTiO₃ that had been previously investigated experimentally using thin film single crystal lamellae. In essence, inherent sources of interfacial capacitance are sometimes evident, and sometimes not.

While this conclusion helps to ameliorate apparent contradictions in the literature, it is uncomfortably convenient: intrinsic dead layers appear to exist in all cases considered, except in those instances where the most careful experiments to look for them have been performed.

Further testing of the general validity of the conclusions drawn from atomistic simulations work is therefore vital. Hence, we herein present new experimental data from Pt/SrTiO₃/Pt single crystal thin film capacitor structures. These were made using the same techniques as had been used previously to unequivocally verify almost bulk-like behaviour in BaTiO₃ single crystal lamellae with Pt electrodes.\(^{(2)}\) We find that that unlike the BaTiO₃ study, thin single crystal lamellae of SrTiO₃ demonstrate significant suppression in permittivity, exactly as predicted by Stengel and Spaldin in 2006;\(^{(3)}\) this lends great confidence to the validity of the more recent conclusions made by Stengel, Vanderbilt, and Spaldin in 2009.\(^{(4)}\)

The capacitor device structures tested are illustrated schematically in Figure 1. The processing steps involved in making the completed capacitors are discussed in detail elsewhere.\(^{(2)}\) However, a brief summary is as follows: lamellae of SrTiO₃ (~13 μm × ~6 μm × ~300 nm) were cut using a single beam focused ion beam microscope (FIB) in much the same manner as would routinely be used for making specimens for transmission electron microscopy investigation. After machining, each lamella was lifted and placed onto a clean MgO single crystal carrier. Thermal annealing at 700 °C in an oxygen atmosphere recovered ion beam damage, and insured that oxygen vacancy point defects were kept to a minimum (the effects of which have been the topic of another recent relevant study\(^{(29)}\)). A thin film of Pt was then sputter-coated on top, and the electrodes and contact pads patterned again using FIB. A replica “dummy” structure was made without the SrTiO₃ lamella to allow background circuit capacitance to be measured directly, and subtracted from the overall signal.

The capacitance as a function of temperature for both the SrTiO₃ lamella, and the bulk crystal from which it had been cut, are presented in Figure 2a. Absolute capacitance values have been normalized to allow a useful comparison to be made. What is immediately apparent is that the dynamic range in permittivity shown by the lamella (increasing by a factor of ~3.5 from room temperature to 10K) is significantly reduced compared to that of the bulk crystal (increasing by a factor of ~150 between room temperature and 10K). When a similar analysis is done for BaTiO₃ (Figure 2b), there are only fractional differences in the dynamic ranges of the permittivities between the lamella and bulk. In other words the changes in permittivity seen in bulk are dramatically suppressed in the Pt/SrTiO₃/Pt thin lamellar capacitor structures, but are relatively unchanged in the Pt/BaTiO₃/Pt thin lamellar structures.

Suppression of permittivity peaks is a characteristic of dead layer interfacial capacitance. It arises because a key diagnostic of interfacial dead layers is that they should act electrically in series with the bulk-like dielectric material found at the heart of the capacitor structure, away from the dielectric-electrode boundary. Thus the behaviour of thin film capacitors is frequently accurately described by a “series capacitor model”:\(^{(1,15–20,30)}\)

\[
\frac{1}{C_{\text{observed}}} = \frac{1}{C_{\text{bulk}}} + \frac{1}{C_{\text{dead layer}}}
\]

(1)

where \(C_{\text{observed}}\) is the capacitance that is measured or observed, \(C_{\text{bulk}}\) is the capacitance expected if the thin film capacitor were to behave in a bulk-like manner, and \(C_{\text{dead layer}}\) is the capacitance associated with the interfacial dead layer, often found to be almost

![Figure 1. Schematic illustration of the geometry used for measuring the capacitance of thin single crystal lamellae (~300 nm thick) of both SrTiO₃ and BaTiO₃ that had been cut from bulk using a focused ion beam microscope.](image)

![Figure 2. The capacitance (at 100kHz) as a function of temperature for both the thin lamellae (open circles) and the bulk single crystals (black squares) from which the lamellae had been cut. Capacitance has been normalized to allow the relative dynamic range of permittivity to be easily compared between bulk and the single crystal thin lamellae. As can be seen in (a), the increase in permittivity with decreasing temperature in SrTiO₃ is dramatically suppressed in the thin lamellae. Inset: plot on logarithmic scale. For BaTiO₃, the dynamic changes in permittivity with temperature (b) are of similar magnitude for both the thin lamella and the bulk crystal across the temperature window investigated.](image)
constant with temperature.\textsuperscript{[15]} It should be clear from Equation 1 that if the expected bulklike permittivity dramatically increases, this increase does not fully transfer into the observed capacitance as it is muted to a degree by the constant “dead layer” term. Hence changes in permittivity expected in bulk are suppressed due to the action of the dead layer.

If the series capacitance model is indeed pertinent in rationalizing the reduced dynamic range of permittivities seen in the SrTiO\textsubscript{3} lamella compared to bulk, and the capacitance of the any potential dead layer is assumed to be temperature invariant, then for any given temperature, \( T \), the following relation should hold:

\[
\frac{1}{C_{\text{lamella}}(T)} = \frac{1}{C_{\text{bulk}}(T)} + K
\]

Hence, for a series of temperatures from 10 to 125K (where the relative error in the measured capacitance in the lamella was small), the inverse capacitance of the lamella was plotted against the inverse capacitance measured in the bulk crystal at the same temperature (Fig. 3). This plot showed two key features: firstly, the inverse capacitances of the SrTiO\textsubscript{3} lamella and bulk crystal are linearly related; secondly, by extrapolation of the data, as: \( \frac{1}{C_{\text{bulk}}} \to 0, \frac{1}{C_{\text{lamella}}} \to \) a finite value. Both these observations are consistent with Equation 2, and therefore also with the series capacitance model (Eq. 1). The progressive suppression in permittivity between room temperature and 10K seen in the SrTiO\textsubscript{3} lamellae is therefore entirely consistent with the presence of a dead layer. An exact value for the parasitic capacitance associated with this dead layer is difficult to determine directly from our data; however, if we assume minimal series capacitance suppression at room temperature, then the progressive suppression of capacitance observed on cooling suggests a value for \( 1/K \) (Eq. 2) of approximately 40fF. We can be confident that this arises directly from the thin lamellar capacitor structure, rather than the external circuitry, since the capacitance values measured from the bulk crystal were much higher than those from the thin lamella. Hence, had the series capacitance originated in the circuitry, series addition would have resulted in a much greater suppression of the bulk signal than that from the thin lamella – the opposite of what was observed.

While previous high resolution transmission electron microscopy (HRTEM) work on single crystal lamellae of BaTiO\textsubscript{3} had demonstrated that continuous interfacial layers were not present after thermal annealing, and that effective recrystallization of ion-implant damage had also been associated with gallium expulsion from the ferroelectric\textsuperscript{[31]} it was nevertheless important to establish that structurally obvious interfacial layers were also absent in the specific case of the FIBEd SrTiO\textsubscript{3} lamellae. To this end, single crystal SrTiO\textsubscript{3} lamellae processed identically to that responsible for the data presented in Figure 2a and Figure 3 were cross-sectioned and examined. It was found that the SrTiO\textsubscript{3} lattice remained intact up to the interface with the platinum electrode, and that no interfacial foreign phase or lattice damage, that might have been responsible for the dead layer effects seen dielectrically, were evident (Fig. 4). So far, we have been unable to determine the exact nature of the termination at the dielectric-electrode interface, but this is clearly an important issue for future work, as the predictions made using atomistic simulations modeling appear are likely to be extremely sensitive to the exact nature of this boundary.

In summary, we present critical data which demonstrate that inherent dead layers occur in SrTiO\textsubscript{3} single crystal thin film capacitor structures with platinum electrodes, which do not exist in analogous structures involving BaTiO\textsubscript{3}. This is entirely consistent with recent atomistic simulations predictions\textsuperscript{[25]} and shows that size-related permittivity suppression in thin film ferroelectric devices, due to specific aspects of the electrode-dielectric boundary, can be extremely subtle. Our data supports the concept that it is the detailed nature of the specific bonds formed at the ferroelectric-electrode boundary that dictate behavior when at the nanoscale.

![Image](https://example.com/image1.png)

**Figure 3.** The manner in which the expected increase in permittivity on cooling has been suppressed in the SrTiO\textsubscript{3} thin lamella compared to bulk has been characterized by a linear relationship between the reciprocal of the normalized measured lamellar capacitance, and the reciprocal of the normalized bulk capacitance at a series of temperatures from 10 to 125K. This linear relationship, and the non-zero intercept on the y-axis, implies a parasitic capacitance in series with the bulk. Such “series capacitance” behaviour is often seen as a fingerprint for the presence of a dead layer acting at the ferroelectric-electrode interface. Its presence in the platinised SrTiO\textsubscript{3} lamella capacitor structures, and absence in the equivalent BaTiO\textsubscript{3} lamella capacitors is entirely consistent with recent atomistic simulations predictions.

![Image](https://example.com/image2.png)

**Figure 4.** Transmission electron microscopy of the interface between a single crystal SrTiO\textsubscript{3} lamella and the thin-film platinum electrode. There is no evidence of any obvious continuous interfacial phase or damaged region that could be responsible for the permittivity collapse observed. It therefore appears that the dead layer effect seen in the Pt/SrTiO\textsubscript{3}/Pt single crystal thin-film capacitor structures investigated here is inherent, in contrast to previous results for analogous Pt/BaTiO\textsubscript{3}/Pt structures.
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