Dangling-bond defect state creation in microcrystalline silicon thin-film transistors

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We analyze the threshold voltage shift in microcrystalline Si thin-film transistors (TFTs), in terms of a recently developed thermalization energy concept for dangling-bond defect state creation in amorphous Si TFTs. The rate of the threshold voltage shift in microcrystalline Si TFTs is much lower than in amorphous Si TFTs, but the characteristic energy for the process, which we identify as the mean energy to break a Si–Si bond, is virtually the same. This suggests that the same basic Si–Si bond breaking process is responsible for the threshold voltage shift in both cases. The lower magnitude in microcrystalline Si TFTs is due to a much lower attempt frequency for the process. We interpret the attempt frequency in amorphous and microcrystalline silicon in terms of the localization length of the electron wave function and the effect of stabilizing H atoms being located only at grain boundaries. © 2000 American Institute of Physics. [S0003-6951(00)03631-7]

Threshold voltage shifts in high-quality amorphous silicon thin film transistors (a-Si:H TFTs) are due to the creation of metastable dangling bonds at the silicon/silicon–nitride interface.1,2 It has been shown recently that microcrystalline Si (μc-Si) TFTs deposited by rf-plasma enhanced chemical vapor deposition (PECVD) using the layer-bylayer (LBL) technique have an improved stability against gate-bias stress.3 In this letter, we apply the thermalization energy concept developed for a-Si:H TFTs1 to these microcrystalline (μc-Si:H) TFTs.

The μc-Si TFT is a top-gate TFT consisting of 50 nm intrinsic μc-Si and 300 nm SiN deposited at 250°C. The μc-Si has a grain size of 10–20 nm and the crystalline fraction is between 87% and 98% determined by ellipsometry.3 Figure 1 shows the normalized linear transfer characteristics of the microcrystalline Si TFT, measured at 300 K and with a source-drain potential Vsd of 0.25 V, compared to one of our standard amorphous silicon TFTs and one of our standard n-channel polycrystalline Si (poly-Si) TFTs. The poly-Si TFT is made by low-temperature laser-crystallization, giving 100–200 nm SiO2 layer and ion-implanted p+ contacts. The standard a-Si TFT has a mobility of typically 0.25 cm2/V·s. The field-effect mobility of the μc-Si TFT is about 0.6 cm2/V·s. This rather low mobility is mainly related to the contacts and not the μc-Si bulk. Time resolved microwave conductivity measurements of similar bulk μc-Si films reveal that the material has a mobility of about 10–30 cm2/V·s.4 The poly-Si TFT has a mobility of about 100 cm2/V·s.

In order to take into account the different gate dielectrics, their thickness, and the nonlinear bandtail carrier dependence of the threshold voltage shift,5 the gate bias has been normalized for a constant surface charge \[ q = \varepsilon \varepsilon_0 (V - V_f) / d \] at about \( 5.7 \times 10^{-3} \text{ C m}^{-2} \). For an amorphous silicon TFT with 300 nm silicon–nitride gate insulator, this amounts to about 32 V above threshold.

Threshold voltage shifts can be unified for different stressing times and temperatures by the thermalization energy concept.1 There is a distribution of energy barriers \( E_D(E) \) which can account for the observed nonexponential kinetic behavior. To a first-order approximation after a time \( t \) at a temperature \( T \), all possible defect creation sites with \( E \leq k T \ln(\nu t) \) will have converted into defects. A thermalization energy can therefore be defined by \( E_{\text{th}} = k T \ln(\nu t) \) where \( \nu \) is the attempt-to-escape frequency, the only fit parameter. The attempt-to-escape frequency has been estimated by the optimal overlap of the degradation kinetics for different stressing times and temperatures. Figure 2(a) shows the threshold-voltage shifts as a function of the thermalization energy for the LBL μc-Si TFT. We obtain an attempt-to-

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**FIG. 1.** Normalized transfer characteristics of a top gate layer-by-layer PECVD μc-Si (dash-dotted line), bottom-gate amorphous silicon (dashed line), and top-gate laser crystallized poly-Si TFTs (solid line).
escape frequency of about \( \nu = 5 \times 10^6 \, \text{s}^{-1} \) for the optimal overlap.

In comparison, a-Si:H TFTs have a more than three orders of magnitude higher attempt-to-escape frequency of about \( \nu = 10^{10} \, \text{s}^{-1} \). Furthermore, this seems to be a unique value for all a-Si:H TFTs. Stannowski et al.\(^6\) measured hot-wire deposited bottom-gate \( \mu c \)-Si TFTs and also found \( \nu = 10^{10} \, \text{s}^{-1} \). The poly-Si TFT exhibits only a very small threshold voltage shift, and particular care is needed to eliminate any charge injection component, but by fitting the data using the same thermalization energy concept, we obtain \( \nu = 10^3 \sim 10^6 \, \text{s}^{-1} \). The high uncertainty in \( \nu \) results from the very low absolute threshold voltage shift of about 1.7 V after \( t = 2 \times 10^5 \, \text{s} \) at 180 °C.

The derivative of the threshold voltage shift with respect to the thermalization energy represents the probability distribution of the energy barrier for defect creation. By fitting the data with a stretched hyperbola fit,\(^2\) one can determine the two relevant parameters \( E_A \) and \( kT_0 \). \( E_A \) is related to the maximum of the probability distribution and \( kT_0 \) to its width.\(^3\) \( E_A \) is about 1.07 eV for the LBL \( \mu c \)-Si TFTs [Fig. 2(b)]. However, the stretched hyperbola does not fit well for low thermalization energies. We believe that this is due to charge injection in the SiN gate dielectric, which has not been optimized for microcrystalline Si TFTs. However, it has a negligible effect on the fit parameters. The fit parameter \( E_A \) is similar to that of amorphous silicon, which is typically between 0.92 and 1.02 eV depending on the material properties.\(^4\) Note that the higher stability for the LBL \( \mu c \)-Si results mainly from the fact that \( \nu \) is more than three orders of magnitude lower. Stannowski et al.\(^6\) report a maximum of about 1.07 eV for their hot-wire (HW) \( \mu c \)-Si TFTs.

We summarize the stability data in Table I. These results indicate that the defect creation mechanism in a-Si:H, LBL \( \mu c \)-Si, and HW \( \mu c \)-Si are similar since the typical energy barrier is virtually the same (\( E_A \approx 1 \) eV). In a previous publication we showed that the typical energy barrier for defect creation, in \( \mu c \)-Si TFTs is related to the intrinsic stress in the silicon layer.\(^5\) We concluded that the breaking of a Si–Si bond is the rate-limiting step for defect creation. The results in this letter suggest that Si–Si bond breaking is responsible for the threshold voltage shift, in both a-Si and \( \mu c \)-Si TFTs. For the poly-Si TFT, a maximum in the derivative of the threshold voltage shift is not detectable, so if \( E_A \) exists, it must be higher than 1 eV. From defect creation theory,\(^6\) we expect a very sharp maximum since \( kT_0 \) is presumably very small due to the high mobility. The maximum of the probability distribution \( E_{\text{max}} \approx E_A - kT_0 \ln(2) \) may be then around 1.1 eV, which is beyond our maximum measurement time at the highest temperature for \( \nu = 10^6 \, \text{Hz} \), i.e., higher than \( 2 \times 10^5 \, \text{s} \) at 180 °C.

The key question is, why is there a different attempt-to-escape frequency for the LBL \( \mu c \)-Si and the poly-Si TFTs on the one hand and the a-Si:H and the HW \( \mu c \)-Si TFT on the other hand. Let us first address the question: “what is the attempt-to-escape frequency?” The attempt-to-escape frequency is the probability that an electron attempts to break the bond. Of course, the bond does not always break during each attempt and to first order, only the Boltzmann fraction with energies higher than \( E_A \) will succeed. For a typical deep defect in the gap where the electron is localized on the bond, the attempt-to-escape frequency of a bond breaking event is about the phonon frequency, typically about \( 10^{12} \, \text{s}^{-1} \). However, an electron in the band tails in amorphous silicon is delocalized over a few atoms, thus the deep defect attempt-to-escape frequency is reduced by the probability that an electron is located on the bond. Since the localization length of an electron in the band tails of amorphous silicon is about 10–20 Å,\(^7\) the probability in three dimensions is reduced by about a factor of 1000, leading to attempt-to-escape frequencies of about \( 10^{10} \, \text{s}^{-1} \). This is in agreement with the experimental data for a-Si:H TFT as well as the HW \( \mu c \)-Si TFT. The HW \( \mu c \)-Si TFT behaves like an a-Si TFT, because there is an amorphous silicon phase in the active region of the bottom gate TFT.\(^6\) The LBL \( \mu c \)-Si TFT is a top gate TFT and the situation is different since the active region consists only of crystallites.\(^3\) Here, the bond-breaking event can only occur near the grain boundaries of the crystallites, since within the crystalline grain, a broken bond would not be stable due to the lack of neighboring hydrogen for the stabilization of the broken bond.\(^1\) The electron has to be situated near the grain boundaries to break a bond. For a grain size of typically 10–20 nm the probability that an electron is located on such a bond is about \( 10^{-7} \), leading to an attempt-to-escape frequency of about \( 10^7 \, \text{s}^{-1} \) in agreement

### Table I. Fit parameter \( \nu \), \( E_A \), and \( kT_0 \) for amorphous Si TFT, a bottom gate (BG) hot-wire \( \mu c \)-Si TFT, a top-gate (TG) PECVD \( \mu c \)-Si TFT, and a top-gate laser-crystallized poly-Si TFT.

<table>
<thead>
<tr>
<th></th>
<th>a-Si:H TFT</th>
<th>BG HW ( \mu c )-Si TFT</th>
<th>TG LBL ( \mu c )-Si TFT</th>
<th>TG poly-Si TFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \nu ) (s(^{-1}))</td>
<td>( 10^{10} )</td>
<td>( 10^{10} )</td>
<td>( 5 \times 10^6 )</td>
<td>( 10^6 )–( 10^7 )</td>
</tr>
<tr>
<td>( E_A ) (eV)</td>
<td>0.92–1.02</td>
<td>1.07</td>
<td>( 5 \times 10^6 )</td>
<td>1.07</td>
</tr>
<tr>
<td>( kT_0 ) (meV)</td>
<td>55–88</td>
<td>68</td>
<td>50–60</td>
<td>—</td>
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</tbody>
</table>

FIG. 2. (a) Threshold voltage shift as a function of the thermalization energy for the layer-by-layer PECVD \( \mu c \)-Si TFT [\( \bullet \)]. The attempt-to-escape frequency is \( \nu = 5 \times 10^6 \, \text{s}^{-1} \). The straight line is a fit based on a stretched hyperbola [\( \therefore \)]. The straight line is a fit based on the derivative of a stretched hyperbola.

with the experimental data ($5 \times 10^6 \text{s}^{-1}$). For the larger grain poly-Si, the electron localization length is significantly smaller than the grain size, due to intragrain defects, which lead to electron scattering within the grains. A typical attempt to escape frequency of $3 \times 10^5 \text{s}^{-1}$, would correspond to an electron localization length of 30–80 nm, which is consistent with the expected electron scattering length in laser crystallized poly-Si, with a film thickness of 40 nm.

In conclusion, we have compared the stability of top-gate LBL $\mu$-Si TFTs with amorphous silicon TFTs, poly-Si TFTs, and bottom gate HW $\mu$-Si TFTs. All TFTs exhibit threshold voltage shifts under bias stress, but with different intensity. The barrier for defect creation is about 1 eV for all TFTs except the poly-Si TFT. However, the probability of a defect creation event in top-gate $\mu$-Si TFTs is much lower. We conclude that in both a-Si TFTs and $\mu$-Si TFTs, dangling bonds are created, with a typical energy barrier of 1 eV. We believe that the probability of a defect creation event is related to the electron localization length. This changes from a typical localized state in an amorphous silicon phase (1–2 nm) to the size of the microcrystallites in top gate microcrystalline silicon (10–20 nm), to the electron scattering length (30–80 nm) in large polysilicon grains. We interpret the attempt frequency in amorphous, microcrystalline, and polycrystalline silicon in terms of the localization length of the electron wave function and the effect of stabilizing H atoms being located only at grain boundaries.

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