Heterogeneous Integration of Compound Semiconductors

Oussama Moutanabbir and Ulrich Gösele[†]

Max Planck Institute of Microstructure Physics, 06120 Halle, Germany;
email: moutanab@mpi-halle.mpg.de

[†]Deceased

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

Annu. Rev. Mater. Res. 2010. 40:469–500

First published online as a Review in Advance on April 1, 2010

The *Annual Review of Materials Research* is online at matsci.annualreviews.org

This article's doi:
10.1146/annurev-matsci-070909-104448

Copyright © 2010 by Annual Reviews.
All rights reserved

1531-7331/10/0804-0469$20.00

Key Words

direct wafer bonding, thin layer and nanomembrane transfer, heterodevices, ion-cut, defect engineering

Abstract

The ability to tailor compound semiconductors and to integrate them onto foreign substrates can lead to superior or novel functionalities with a potential impact on various areas in electronics, optoelectronics, spintronics, biosensing, and photovoltaics. This review provides a brief description of different approaches to achieve this heterogeneous integration, with an emphasis on the ion-cut process, also known commercially as the Smart-Cut™ process. This process combines semiconductor wafer bonding and undercutting using defect engineering by light ion implantation. Bulk-quality heterostructures frequently unattainable by direct epitaxial growth can be produced, provided that a list of technical criteria is fulfilled, thus offering an additional degree of freedom in the design and fabrication of heterogeneous and flexible devices. Ion cutting is a generic process that can be employed to split and transfer fine monocrystalline layers from various crystals. Materials and engineering issues as well as our current understanding of the underlying physics involved in its application to cleaving thin layers from freestanding GaN, InP, and GaAs wafers are presented.

INTRODUCTION

CS: compound semiconductor

MOSFET: metal-oxide-semiconductor field effect transistor

ITRS: International Technology Roadmap for Semiconductors

In his recent analysis of the nature of technology, Arthur (1) proposed that all technologies descend from preexisting ones, so the essence of technological progress is based on assembling new combinations of earlier and refined technologies. This concept of combinatorial evolution, as coined by Arthur, is pertinent to the subject of this review, the heterogeneous integration of compound semiconductors (CSs) by wafer bonding and thin-layer transfer. The possibility of incorporating CS-based devices into the traditional Si technologies has sparked a surge of interest motivated by the novel and improved functionalities potentially achievable by this heterointegration (2–35). In this landscape, the much higher charge carrier mobility (as compared with that of Si) and the efficient emission of light by some CSs due to their direct bandgap (as compared with the indirect bandgap of Si) have been the two major driving forces in the development of heterogeneous devices.

Technological Background

For approximately a half-century, device downscaling was the most important strategy for performance enhancement in Si metal-oxide-semiconductor field effect transistors (MOSFETs). However, keeping with this relentless course of miniaturization turns out to be very challenging for the future technology nodes. This is clearly evidenced in the 2007 edition of the International Technology Roadmap for Semiconductors (ITRS), which establishes the technological challenges in the semiconductor industry. For instance, to meet the performance and power requirements for highly scaled MOSFETs at and below the 10-nm gate length, quasi-ballistic operation with enhanced thermal carrier velocity and injection at the source end appears to be necessary. Ultimately, the introduction of new device structures such as high-transport Ge or CS channels on Si may be needed. As shown in **Table 1** (36–41), several CSs have a substantially higher electron mobility compared with Si. This has inspired the development of several non-Si transistors. Starting from the mid-1960s, GaAs was the first CS to be used in the fabrication of MOSFETs (42–45). Several

Table 1 Basic properties at 300 K of some important undoped compound semiconductors[a]: bandgap (E_g), hole mobility (μ_h), electron mobility (μ_e), Young's modulus (E), and Poisson ratio (σ)

	E_g (eV)	μ_h (cm^2 Vs^{-1})	μ_e (cm^2 Vs^{-1})	E (GPa)	σ
C	5.46–5.6	$\leq$1800	$\leq$2200	1050	0.1
Si	1.107	$\leq$450	$\leq$1400	130	0.28
Ge	0.661	$\leq$1900	$\leq$3900	103	0.26
$Si_{1-x}Ge_x$	$1.12–0.41x + 0.008x^2$ for $x < 0.85$; $1.86–1.2x$ for $x > 0.85$	$450–865x$ ($0 \leq x < 0.3$)	$1450–4325x$ ($0 \leq x < 0.3$)	$130.2–28.1x$	$0.28–0.02x$
GaP	2.261	120	200	103	1.1
GaAs	1.428	420	8500	85.9	0.455
GaSb	0.70	1400	7700	63.1	0.33
InP	1.35	150	4500	61.1	0.7
InAs	0.356	460	33000	51.4	0.26
InSb	0.18	850	78000	40.9	0.18
GaN	3.42	$\leq$200	~1400	150	0.23
AlN	6.2	14	300	~340	~0.2

[a]Data compiled from References 36–41. For GaN only, values corresponding to wurtzite structure are shown. For comparison, properties of diamond, Si, and Ge are also shown.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

CSs such as InP, GaAs, GaN, and their ternary and quaternary alloys (InGaAs, InAlAs, AlGaN, InGaP, InGaAsN, AlGaAs, and GaAsSb) as well as SiGe alloys have been used in the fabrication of heterojunction bipolar transistors (46–51). Besides GaAs, GaN (52) and InAs (53) have attracted a great deal of attention in the fabrication of high-electron-mobility transistors (HEMTs). In a more recent development, Intel researchers revealed a novel ultrahigh-speed transistor based on InSb quantum wells on GaAs (54, 55). In spite of the fact that the advantages of CS devices over their Si counterparts were recognized several decades ago, CSs combined with Si were included only in the 2003 and later editions of the ITRS. This is due to the increasing necessity of incorporating non-Si materials into complementary metal-oxide-semiconductor (CMOS) transistors to boost their performance and to enhance their energy efficiency.

HEMT: high-electron-mobility transistor

CMOS: complementary metal-oxide-semiconductor

Because of its indirect bandgap, crystalline Si is a poor light emitter. To enhance the emission of light from Si, investigators have made several efforts to manipulate Si on the nano- and quantum scales (56–58) and to exploit its nonlinear optical properties (59–61). However, it is unlikely that these devices will outperform their CS counterparts, which currently provide state-of-the-art optoelectronic devices for the telecommunication market. Therefore, the marriage of CS photonic devices and Si integrated circuit technology to achieve an efficient on-chip light emitter remains a serious alternative to supplying the light from a light source outside the actual chip (analogous to the supply of electrical energy from a battery). Successful fabrication of lasers, photodetectors, amplifiers, and modulators on Si was recently demonstrated by integrating CS (mainly InP, GaAs, GaN, and SiGe) thin films, quantum wells, and dots on Si substrates (7–9, 15–23, 31, 32, 62–64).

In addition to photonic, electronic, and optoelectronic applications, CSs are important for other application areas such as high-efficiency photovoltaic cells (65–70), biosensing (35, 71–73), and spintronics (74, 75). Well-controlled integration processes of CS-based structures and devices may impact these areas as well by providing an additional degree of freedom in the fabrication and design, enhancing the performance and reducing the fabrication cost.

Challenges

The integration of CSs with logic-chip technology presents several serious challenges. At the device level, for instance, the realization of reliable CS-based transistors is still facing major difficulties such as finding a high-quality gate insulator (unlike Si, oxides of CSs are of poor quality, contain defects, and trap charges), forming low-resistivity contacts, and fabricating transistors that efficiently conduct holes (*p*-type transistors). The state-of-the-art developments on these issues were recently compiled in a complete issue of the *MRS Bulletin* (11). Obviously, the optimal integration process must be economically viable for CMOS applications. This can happen only if CS-based devices are integrated onto large Si wafers, given the fact that it is currently not possible to produce CS wafers with diameters close to what is possible for Si (i.e., a diameter of 300 mm/12 inches or more in the near future). Over the years, there have been major efforts in the development of reliable and cost-effective processes for CS/Si integration. In general, one can distinguish between three different approaches: (*a*) epitaxy-based, (*b*) wafer bonding–based, and (*c*) hybrid (i.e., involving the use of both epitaxy and wafer bonding) heterointegration processes. Lattice parameter, thermal expansion coefficient, and crystal structure mismatches remain the most influential parameters in these processes. The stability of the resulting heterostructure against high-temperature treatments is also a very critical parameter that should be considered when subsequent processing steps involve high-temperature treatment. The limitations imposed by these parameters and their influence on various heterointegration processes are discussed below. In the next section, we briefly describe the progress in heterogeneous integration by direct epitaxy. The remaining sections focus on wafer bonding and thin-layer transfer, with an emphasis on the

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

application of the ion-cut process to cleave freestanding GaN (fs-GaN), InP, and GaAs wafers. We address materials and engineering issues as well as our current understanding of the basic mechanisms involved in this heterointegration process.

fs-GaN: freestanding GaN

REMARKS ON HETEROINTEGRATION BY EPITAXY

Figure 1 displays the variations, relative to Si(001), of the lattice parameter (a) versus thermal expansion coefficient (α) of several CSs. We note that most CSs exhibit a strong lattice and thermal mismatch with Si. For instance, the lattice (thermal) mismatch of GaAs, InP, InSb, and GaN (wurtzite) with Si is in the order of 3.9% (128.1%), 8.0% (73.1%), 19.5% (106.5%), and 41.3% (115.0%), respectively. These incompatibilities strongly limit the quality of CS epitaxial layers grown on Si substrates. Heteroepitaxial layers of these materials on Si suffer from a large density of dislocations, many antiphase domains, and autodoping effects (76). These defects can affect both the carrier mobility and the leakage current in the devices. To circumvent these difficulties, several strategies have been pursued. A two-step growth process using a buffer layer deposited at a relatively low temperature (≤300°C) was proven to be efficient in reducing dislocation density and eliminating antiphase domains in the GaAs/Si system (77, 78). However, this approach is not as effective for larger mismatch systems such as InSb/Si (79).

Alternatively, growth on a metamorphic composite buffer leads to relatively higher quality CS layers. The role of this buffer layer is to reduce antiphase domains, to bridge lattice constants, and to relax strain energy and gliding dislocations. For example, the recent demonstration of $In_{0.7}Ga_{0.3}As$

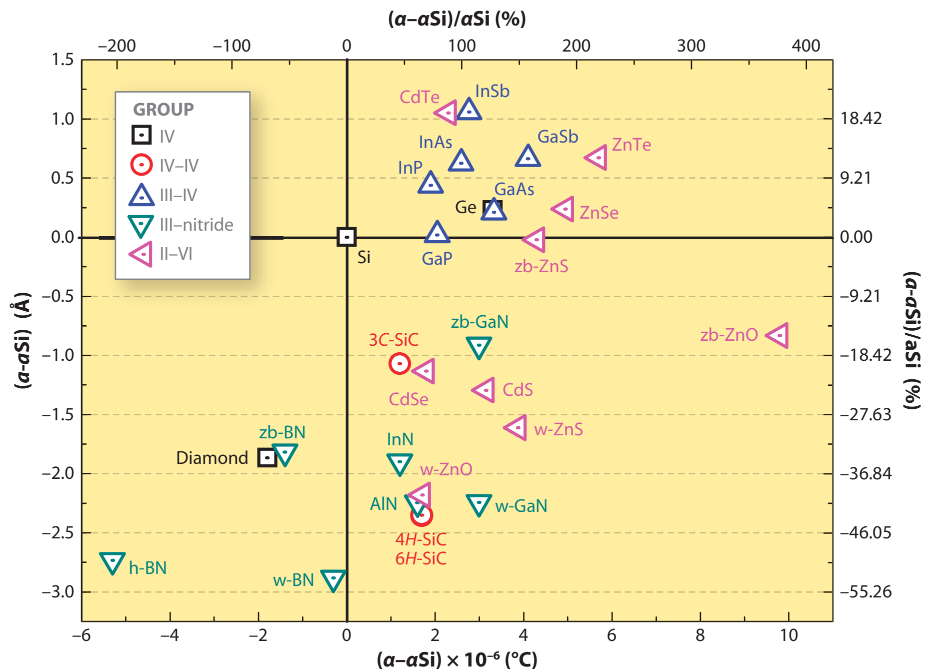

Figure 1

The variations relative to Si(001) of the lattice parameter (a) versus the thermal expansion coefficient (α) of several compound semiconductors (CSs). w, wurtzite; zb, zinc blend; h, hexagonal. The values are compiled from References 36–41.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

quantum well transistors on Si was achieved using an $In_xAl_{1-x}As$ graded buffer deposited on a GaAs buffer layer with a total thickness of ~1.3 μm (12). Similarly, InSb quantum well–based high-speed transistors were fabricated using a 3-μm-thick $Al_xIn_{1-x}Sb$ layer grown on a 200-nm $Al_yIn_{1-y}Sb$ layer deposited on a GaAs substrate (54, 55). However, despite this progress in improving the quality of CS-on-Si films, the obtained heterostructures following the aforementioned processes still contain a relatively high density of defects at the interface with the Si substrate. The use of microchannel lateral epitaxy (80, 81) can produce higher-quality layers (82) but requires an additional well-controlled patterning of the substrate. Another promising approach is the use of a Ge layer on Si as a template for the growth of a GaAs buffer and device layers (83, 84). The lattice mismatch between Ge and GaAs is only ~0.28%, which warrants high-quality crystalline GaAs layers. Nevertheless, the obtained heterostructure contains a defective interface generated to relieve the misfit strain due to the ~4% mismatch between the Si and Ge lattices, unless bonding-based approaches are employed to fabricate the Ge/Si template wafers (13, 14). The formation of a thin Ge layer on Si by Ge condensation is also a possible option (85). Obviously, the use of high-quality Ge/Si templates can allow for the growth of high-quality GaAs layers but is not a solution for most other CSs because of their lattice mismatch with Ge.

VLS: vapor-liquid-solid

Another epitaxial variety for the heterogeneous integration is the growth of self-assembled CS nanowires on Si. Among all synthesis methods, the vapor-liquid-solid (VLS) process is the most successful in generating high densities of monocrystalline nanowires (86). In this process, the growth of nanowires is accomplished via a liquid-metal cluster that acts catalytically as the energetically favored site for vapor-phase reactant absorption and, when saturated, as the nucleation site for crystallization and one-dimensional growth. In the early 1990s, Hiruma and coworkers (87, 88) were the first to demonstrate the growth of GaAs and InAs nanowires via the VLS process, using Au as a catalyst. Recently, several groups reported the growth of defect-free monocrystalline CS nanowires on Si (33, 88–91). Although self-assembled nanowires permit the circumvention of lattice and thermal mismatch issues faced in engineered heteroepitaxial layers, it is still premature to predict whether their integration can be successfully achieved at the device level due to numerous difficulties involving control over the size, position, distribution, and orientation of the growing nanowires in addition to the same aforementioned problems faced in CS thin-film device–related processing.

INTEGRATION BY WAFER BONDING

General Remarks

The combination of dissimilar semiconductor materials within the same platform without the need for direct epitaxy can be realized by using wafer bonding and layer transfer technologies. In a first step, the donor and host wafers are tightly joined to form a single entity (92–94). In general, this can be accomplished by following one of the different bonding processes indicated in **Figure 2**. The bonding process is usually chosen depending on the nature of the initial substrates and their tolerance to temperature as well as on the final application. In principle, a variety of materials can be bonded independently of their structure (monocrystalline, polycrystalline, amorphous), their crystallographic orientation, and their lattice parameter. Due to limited space, we do not address the history and fundamental issues of bonding processes but direct the reader to relevant books and review articles (92–99).

In general, the bonding of CSs can be accomplished through one of two generic bonding processes. The first one is to directly bond the wafers without using an intermediate layer. Using a microcleanroom setup, Lehmann et al. (100) obtained bubble-free and highly stable direct

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

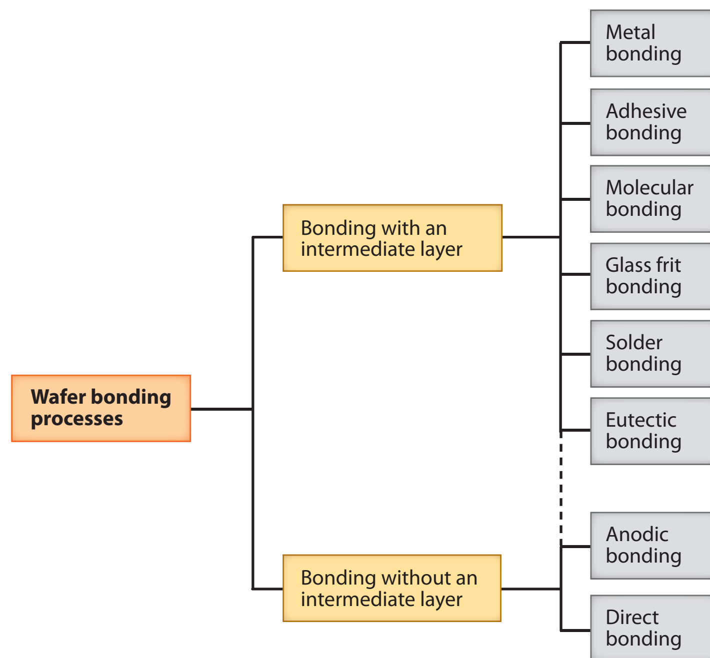

Figure 2

Wafer bonding processes currently used in semiconductor technology. The dashed line denotes that anodic bonding can also be achieved using an intermediate layer.

bonding of InP and GaAs wafers to bare Si. Due to direct thermal contact between the wafers, this direct bonding provides good thermal conductivities. However, the formation of interface states can be harmful and may significantly influence the bending of the energy bands (101). Surface conditioning and wafer bonding in ultrahigh vacuum (UHV) environment can alleviate this problem and produce nearly structurally and chemically abrupt interfaces, as demonstrated for GaAs/Si (see **Figure 3*a*** and Reference 102), SiC/Si (103), and GaN/Si (104). An additional and serious complication in the direct bonding of dissimilar materials results from the significant difference in the thermal expansion coefficients (**Figure 1**). Such thermal mismatch generates stress during annealing at temperatures usually higher than 600°C, which is required to strengthen the bonded interface. Pasquariello et al. (104) presented a detailed study of the evolution of the structural properties of InP directly bonded to Si as a function of increasing temperatures. They found that annealing below 300°C does not affect the bonded pair, whereas annealing above this temperature generates volume dislocations in InP. However, the density of dislocations in this case remains much lower than in direct heteroepitaxy. The increase in temperature (>400°C) produces voids at the interface, which are attributed to the nucleation of In droplets. In general, the interfacial voids, due to the material decomposition and/or to the generated gas by-product, can be eliminated by patterning in-plane channels at the interface (104) or vertical channels in the host substrate (105). The evident remedy to this thermally induced CS degradation would be to restrict the direct bonding and the interface strengthening to low temperatures. In this regard, Tong et al. (106) presented a promising method by which strong InP/Si direct and stable bonding is obtained at relatively low temperature. Their method is based on the use of B_2H_6 plasma to condition the surfaces, followed by an HF dip prior to contacting and bonding the wafers at room temperature. The interface energy reached the InP fracture surface energy of 630 mJ m^{-2} after

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

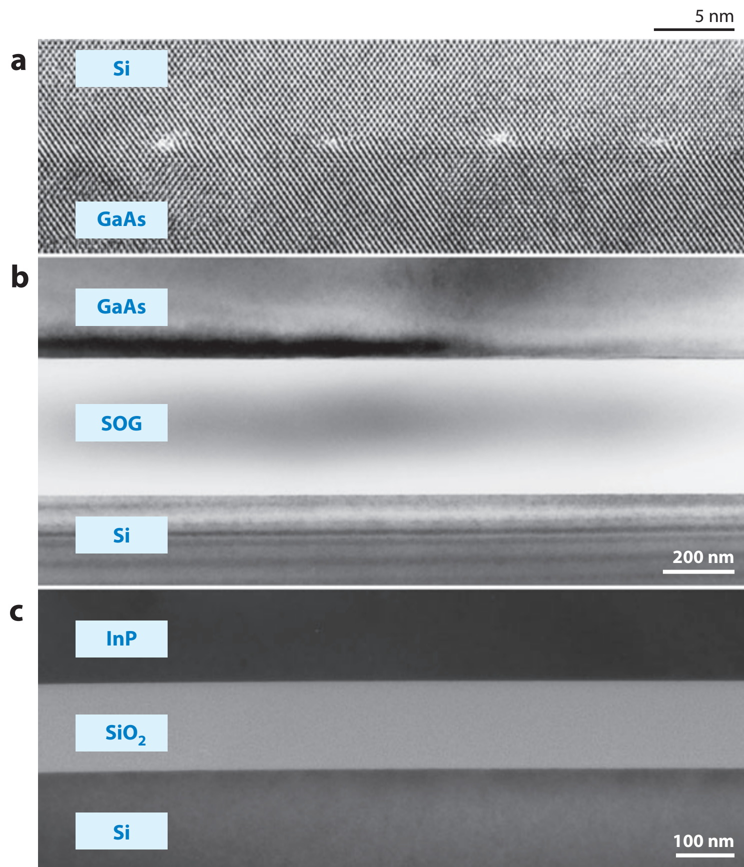

Figure 3

(*a*) High-resolution cross-sectional transmission electron microscopy (TEM) image of a Si/GaAs interface directly bonded in ultrahigh vacuum and annealed at 850°C for 30 min. Adapted from Reference 102. (*b*) Cross-sectional TEM image of GaAs bonded to Si by use of a spin-on-glass (SOG) layer at 160°C. Image courtesy of M. Alexe. (*c*) Cross-sectional TEM image of a high-temperature-compatible InP layer transferred onto Si by use of a plasma-enhanced chemical vapor deposition (PECVD) SiO_2 interlayer.

annealing at 200°C. However, the formation of an amorphous B-rich interfacial layer may be problematic for specific applications of this process.

The second generic process is bonding via an intermediate layer, which can be dielectric [e.g., native oxide, SiO_2, spin-on-glass (SOG), or Si_3N_4], metal, or polymer. This type of bonding significantly reduces the thermal budget as well as the interfacial irregularities (e.g., roughness or waviness) (107–110). For instance, the use of SOG as the bonding layer leads to good-quality bonding of GaAs wafers to Si wafers upon annealing at a temperature as low as 200°C (**Figure 3*b***). However, in some cases (e.g., those involving SOG or polymers), the use of an intermediate electrically insulating layer comes with a restriction in the postbonding thermal processing and in the power-handling capabilities of the bonded pair because of the typically low thermal conductivity of such intermediate layers. A high-temperature-compatible heterostructure can be fabricated by the use of a SiO_2 layer deposited on the CS wafer by, e.g., plasma-enhanced chemical vapor deposition (PECVD) (**Figure 3*c***). Here bonding to a Si wafer becomes similar to the well-controlled

SOG: spin-on-glass

PECVD: plasma-enhanced chemical vapor deposition

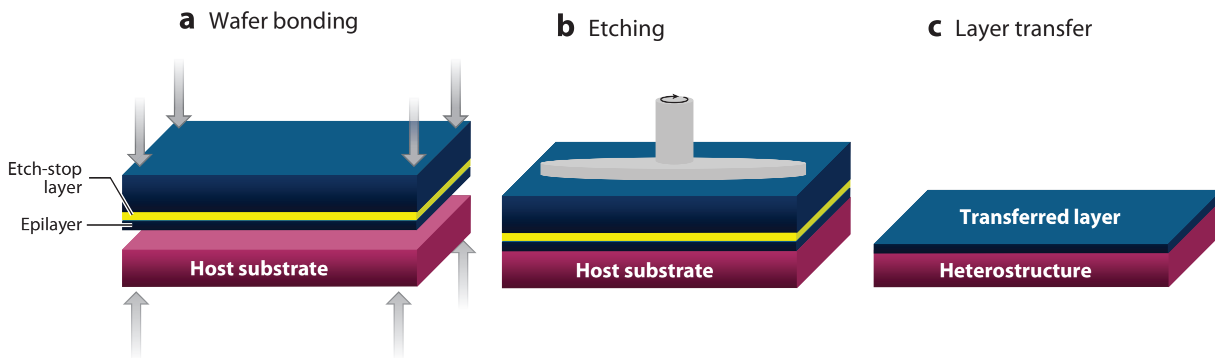

Figure 4

Schematic illustration of thin-layer transfer by combining epitaxy, wafer bonding, and mechanical thinning. For better control of the thin-layer thickness, a lattice-matched etch-stop layer is deposited onto the seed substrate. The transferable layer is then grown epitaxially on this etch-stop layer.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

hydrophilic bonding of Si (93, 110). Bonding of dissimilar wafers can also be performed via a metal as the interfacial layer (111). Bonding in this case is based on the isothermal solidification process, in which the surfaces to be bonded are capped with high- and low-melting-point metals. Bonding takes place by annealing at a temperature between the two melting points, which leads to the formation of an intermetallic alloy. Recently, Bickford et al. (112) demonstrated the bonding of GaAs to Si by using In as the low-melting-point metal and Pd as the high-melting-point metal.

Layer Transfer by Mechanical or Chemomechanical Thinning

The second step in wafer bonding–based heterointegration consists of releasing a thin layer from the donor wafer after the bonding process. A direct approach is to mechanically grind, lap, and polish one of the wafers until only a desired film thickness remains. Using this approach, Huang et al. (113) fabricated GaAs-on-insulator substrates. One of the limitations of this process is the deterioration of the layer uniformity for a thickness below 10 μm. This can possibly be dealt with by an additional thinning step using a plasma-based procedure, which produces a thickness uniformity of approximately 10 nm in the case of Si-on-insulator (SOI) wafers (93). A more reliable alternative is the introduction of an etch-stop layer before bonding (**Figure 4**). Using this procedure, Bowers and coworkers (23, 114) successfully demonstrated the transfer of a thin layer of InP (up to 150 mm in diameter) onto a Si wafer. In this process, a *p*-doped $In_{0.53}Ga_{0.47}As$ lattice-matched layer grown on InP is introduced as the etch-stop layer. After the epitaxial growth of a thin layer of InP and bonding to the Si host substrate, the handle InP wafer is selectively etched in a $HCl:H_2O$ (3:1) mixture. Similarly, GaAs and GaSb epitaxial thin layers are transferred onto a different host substrate by using AlAs (or AlGaAs) (34, 35) and InAsSb (115) as etch-stop layers, respectively. The obvious drawback in this process is the cost involved in losing the complete starting CS wafer, which is not affordable for very expensive materials, such as fs-GaN.

Layer Transfer by Mechanical Lateral Cleaving

To save in material costs, preservation of the device wafer or seed substrate to reuse it for the transfer of several thin layers has been driving the development of various alternative processes. **Figure 5** displays a schematic illustration of a thin-layer-transfer process in which an epitaxial layer

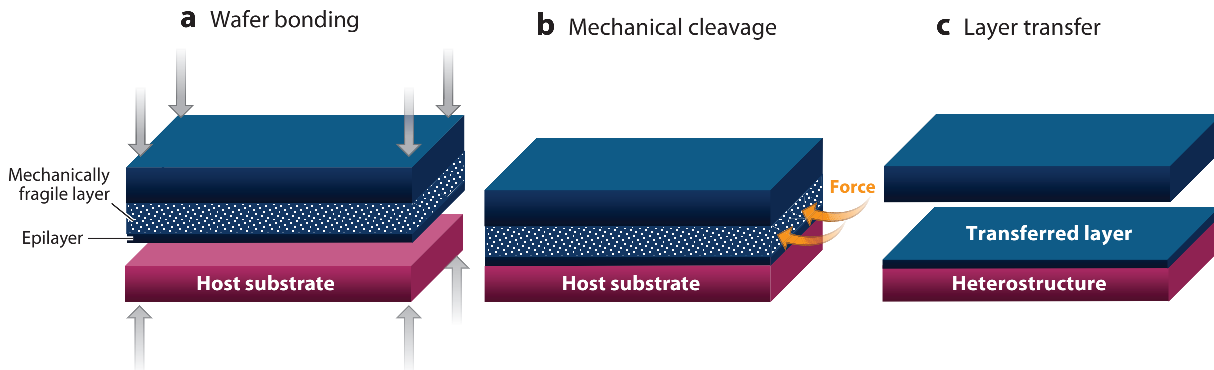

Figure 5

Schematic illustration of thin-layer transfer by mechanical splitting. The process consists of the introduction of a mechanically fragile layer, on top of which the layer to be transferred is grown epitaxially. After bonding, layer transfer is achieved by crack propagation through the mechanically fragile layer following the application of a mechanical force at the edges of the bonded wafers.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

is mechanically cleaved from the donor wafer after bonding to the host wafer. McClelland et al. (81) pioneered CS layer transfer using this mechanical splitting. In their process, named CLEFT (cleavage of lateral epitaxial films for transfer), a few-micrometer-thick GaAs layer grown by lateral epitaxy on a GaAs substrate partly covered with a SiO_2 layer is bonded with epoxy to a 250-μm-thick glass substrate. The back side of the GaAs substrate is in turn bonded with wax to a 5-mm-thick glass substrate, which acts as cleaving support. The epitaxial GaAs thin film is cleaved by exerting a mechanical force via use of a metal wedge inserted between the two glass substrates. The seed GaAs substrate can be reused after removing it from the glass substrate. The transfer of GaAs films with areas of several square centimeters was demonstrated through use of this approach. Better control of the cleavage and transfer of larger areas can be obtained by introducing, prior to bonding, a mechanically fragile layer between the handle wafer and the layer to be transferred (**Figure 5**). The established process developed by researchers at Canon (116) in the mid-1990s for the transfer of a thin, single-crystalline Si layer is the use of an embedded porous Si layer as the mechanically weak splitting region. In this process, commercially known as ELTRAN (epitaxial layer transfer), two porous layers with different pore diameters are formed by anodization of the seed wafer followed by the growth of a thin epitaxial Si layer. After dry oxidation and bonding, the application of a mechanical force (e.g., a water jet) at the edge of the bonded pair leads to splitting parallel to the surface close to the interface between the two porous layers. SOI substrates with diameters up to 300 mm were fabricated using this process (117). However, in spite of the demonstration of anodization-induced pore formation in many CS materials (118) and the growth of good-quality epitaxial layers on porous CSs (119), studies of the feasibility of this process of thin-layer transfer for CSs are absent in the literature.

Layer Transfer by Selective Chemical Undercutting

In addition to mechanical splitting, thin-layer transfer can also be achieved by selective lateral chemical etching of a sacrificial layer introduced between the handle substrate and the layer to be transferred, as illustrated in **Figure 6**. Konagai et al. (120) first demonstrated this chemical undercutting, termed peeled film technology. On the basis of the excellent selectivity of $Al_xGa_{1-x}As$ alloys in hydrofluoric acid (with respect to GaAs), these investigators succeeded in splitting

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

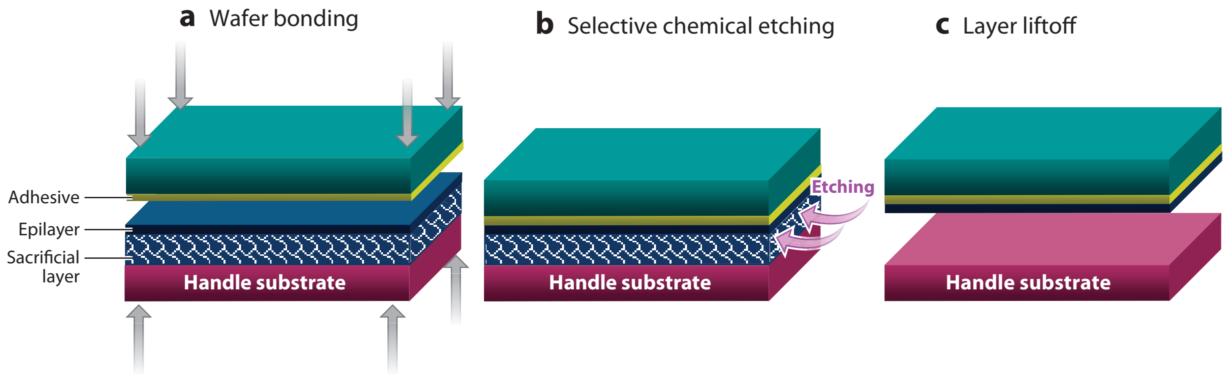

Figure 6

Schematic illustration of thin-layer transfer by undercutting using selective chemical etching. The process consists of the introduction of a lattice-matched sacrificial layer, on the top of which the layer to be transferred is grown epitaxially. After direct bonding (or gluing by using an adhesive), the obtained heterostructure is immersed in a chemical solution that selectively etches the sacrificial layer. Acceleration of the etching process as well as an increase in the area of the transferred layer can be achieved by drilling microscopic holes in the handle substrate.

30-μm-thick GaAs solar cells. Yablonovitch et al. (121) later optimized and improved this procedure. In their process (121), the GaAs-based layer to be transferred, which may also contain processed devices, was epitaxially grown on a thin AlAs etch-stop layer, which in turn was epitaxially grown on the GaAs handle wafer. The whole structure was attached to a wax-type transfer substrate, and then the AlAs layer was etched away laterally in hydrofluoric acid. The released thin layer could be attached to a handle wafer (e.g., Si) by bonding and removal of the transfer substrate. This epitaxial liftoff (ELO), however, is limited to the transfer of layers with a lateral dimension of a few centimeters due to the relatively slow lateral etch rate (~100 μm h^{-1}).

THE ION-CUT PROCESS

Basic Aspects

An elegant way to cleave a semiconductor thin layer is to implant, under well-controlled conditions, H and/or He energetic ions to create a mechanically weak zone a few hundred nanometers below the surface of the donor wafer, as illustrated in **Figure 7**. The implanted wafer is then bonded to a handle wafer, and the obtained pair is subjected to thermal annealing at a temperature in the 200–500°C range. During annealing, the interaction of the implanted species with the radiation damage acts as an atomic scalpel, producing extended internal surfaces in terms of pressurized microcracks parallel to the bonding interface. This leads to the splitting and transfer of a thin layer with a thickness roughly equivalent to the implantation depth. However, the layer transfer takes place successfully only if the donor/handle wafer bonding interface remains stable during thermal annealing. In contrast to the processes described in the previous sections, layer transfer can be achieved by directly splitting the donor wafer without the need of an additional epitaxy step. This ion-cut process-–commercially known as Smart-Cut^{TM}—was developed in the mid-1990s (122) and is currently used for the industrial production of SOI and Ge-on-insulator (GOI) wafers with diameters up to 300 mm (122–124). Thin layers from inorganic crystals other than semiconductors can also be cleaved using this process (125–127). Another variety of the ion-cut process—known as ion slicing—exploits the implantation-induced change in the chemical properties to achieve

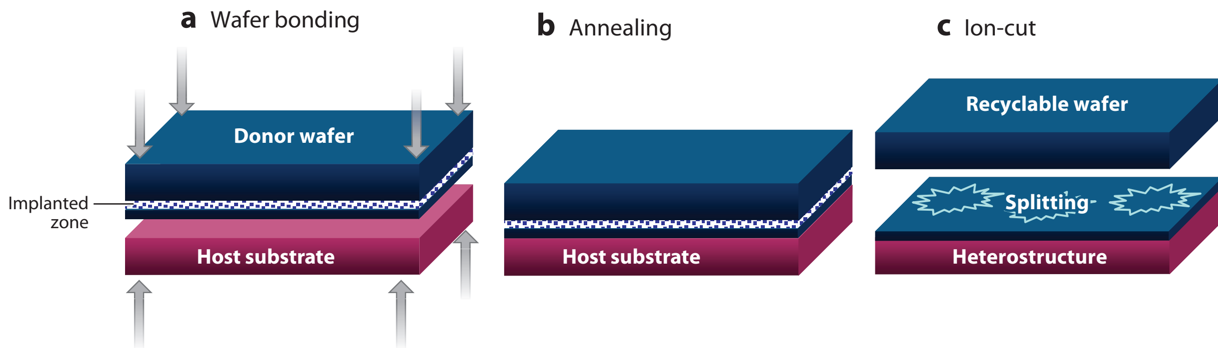

Figure 7

Schematic illustration of thin-layer transfer by the ion-cut process. A mechanically weak zone is produced below the surface of the donor wafer by using H and/or He ion implantation. After bonding and annealing, subsurface microcracking takes place, leading to the lateral cleavage of the whole substrate around the implantation depth parallel to the surface.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

thin-layer release through the selective chemical etching of the damage zone, usually without the need for high-temperature annealing (128–131). Besides the implantation of monoenergetic ion beams, plasma immersion ion implantation can also be used in the ion-cut process (132). These successful applications have led to a sharp increase in the experimental and theoretical studies of H (and He) interactions with implantation-induced defects and their thermal behavior in order to understand in detail the fundamental mechanisms responsible for layer splitting (133–135). A few works have also been devoted to the investigation of the basic mechanisms underlying layer splitting in some CSs (136–142). For typical implantation energies of up to approximately 200 keV, annealing of the implanted wafers without the presence of a bonded second wafer usually leads to blistering. However, if the implantation depth is large enough (e.g., for an ion energy of ∼1–4 MeV or higher), the upper layer acts as a stiffener, which leads to splitting without the need for a handle wafer. This technology is based on a process developed by Reutov & Ibragimov (143) in 1983 in Russia. Silicon Genesis Corporation improved this technology and has been exploiting it in the fabrication of 17-μm-and-thicker Si foils for solar energy applications (144). It would be fundamentally and technologically interesting to explore the feasibility of this process for CSs as well. Here one of the fundamental questions is to establish the critical thickness at which liftoff can occur for a given material. However, the obvious technological challenge remains the development of cost-effective high-energy implanters for large substrates.

As mentioned above, for an ion energy of ≤200 keV and in the absence of the handle wafer, the surface of the implanted donor wafer after an appropriate thermal annealing procedure becomes bookmarked with dome-shaped blisters as well as craters left by the exfoliation of some of these blisters. Panels *a–c* of **Figure 8** show typical blisters and craters observed under ion-cut conditions. This phenomenon is observable in all crystalline materials containing several atomic percent H and/or He. Whereas this blistering is detrimental for materials used in nuclear fission and fusion reactors, the control and the exploitation of this phenomenon are highly desirable in semiconductor technology. From a thermodynamics viewpoint, the limited solubility of the implanted species in most materials provokes their segregation into cavities that grow and coalesce at high temperatures (145, 146). Thus, the blisters appear due to surface deformation caused by the gas pressure in the cavities and coalescence of many microscopic cavities. The interesting physics question is by which atomic processes ion cutting takes place. Yet there is no universal answer that is valid for all materials of technological interest.

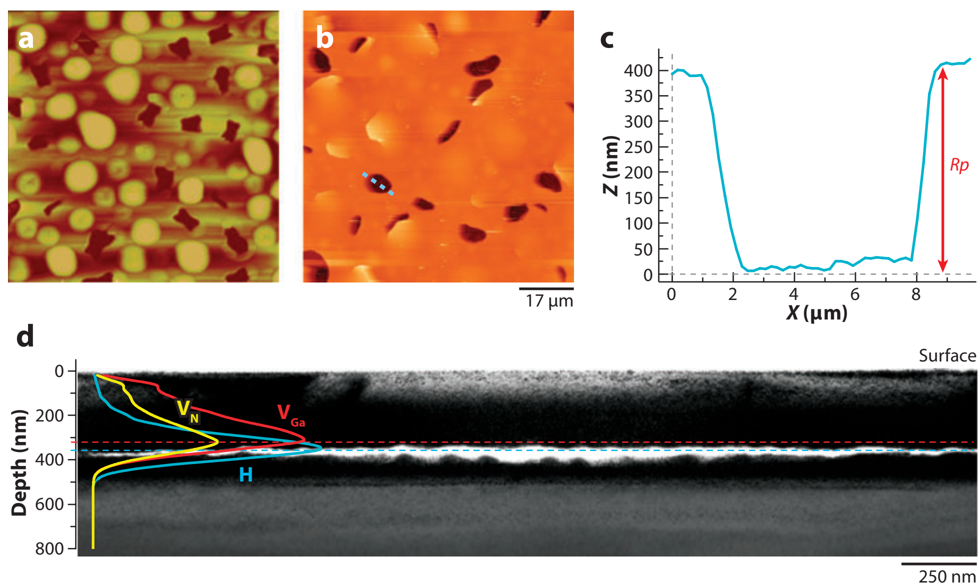

Figure 8

(*a*) A 5 µm × 5 µm atomic force microscopy (AFM) image of a He-implanted Si(001) substrate at 8 keV with a fluence of 1.2 × 10^{17} cm^{-2} and annealed at 550°C. (*b*) AFM image of a H-implanted GaN substrate at 50 keV with a fluence of 2.6 × 10^{17} cm^{-2} and annealed at 600°C. The blue line denotes the region from which the linear scan in panel *c* is taken. (*c*) Profile of a crater shown in panel *b*. *Rp* denotes the projected range of the implanted H ions. (*d*) Cross-sectional TEM image of the sample shown in panel *b*. The depth profiles of H and N vacancy (V_N) and Ga vacancy (V_{Ga}), calculated using the SRIM 2006 program, are superposed onto the image. In this case, the splitting takes place around the H concentration peak.

Understanding the basic mechanisms of H/He diffusion and aggregation up to the formation of microcracks and finally layer splitting is vital for better control of the ion-cut technology. Techniques such as vibrational spectroscopies (147–152), transmission electron microscopy (135, 153), Rutherford backscattering spectrometry in the channeling mode (154–156), X-ray diffraction (157–159), and positron annihilation spectroscopy (155, 160) greatly improved our understanding of the microscopic mechanisms of the ion-cut process, although mainly for Si. These studies have demonstrated the critical role of H vacancy (H-V) complexes and damage-generated stress in the formation of nanoscopic platelets and voids in Si immediately after implantation. Thermal annealing induces an increase in open-volume defects parallel to a rearrangement in H-V complexes characterized by a collapse of multivacancy complexes and the persistence of (or even an increase in) highly passivated monovacancies. Despite the absence of conclusive evidence, it is generally assumed that the formation and trapping of H_2 molecules trigger the observed microstructural transformations. Annealing above a critical temperature leads to a relaxation of the internal strain by subsurface microcracking, as shown in **Figure 8*d***. These extended internal surfaces form roughly around the projected range, but their exact depth varies slightly, depending on the implanted fluence due to change in the fracture mechanics (154, 161). Chabal and coworkers (136) presented a detailed study of the thermal evolution of H-defect vibrational modes leading to splitting and the transfer of thin InP layers. Their measurements were carried out on 80-keV H^+-implanted InP substrates (fluence = 1 × 10^{17} H^+ cm^{-2}) (102) that were annealed at various temperatures between ~100 and 400°C. The authors found that in the as-implanted state, H is distributed predominantly in isolated point-like configurations, with a smaller concentration of

H-V: hydrogen vacancy

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

extended defects with uncompensated dangling bonds. During thermal activation, H is detrapped from point defects and is recaptured at the peak of the distribution by free internal surfaces in dihydride configurations. The authors speculate that, at higher temperatures and immediately preceding exfoliation, rearrangement processes lead to the formation of H clusters and molecules (136). The identification of the thermoevolution of H-defect complexes involved in the ion cutting of other CSs remains an open challenge.

CMP: chemomechanical polishing

Ion Cutting of InP and GaAs

The major challenge in the application of the ion-cut process to transfer CS thin layers onto a foreign substrate remains the elimination of the thermally induced interfacial stress caused by the difference in the thermal expansion coefficients (**Figure 1**). Therefore, achieving a mechanically strong bonding interface at relatively low temperatures is a prerequisite not only to circumvent thermal stress issues but also to avoid surface blistering at the bonding interface that takes place at temperatures as low as 250°C. Additionally, the implantation temperature is particularly critical in the ion cutting of InP and GaAs. For efficient splitting, some reports have suggested that implantation should be performed at temperature windows of 160–250°C for GaAs and 150–250°C for InP (162). In contrast, other researchers have demonstrated that implantation in the −20–20°C range leads to successful InP cleaving (163). These contradictory reports on the optimal implantation temperature may be due to differences in other implantation parameters and process conditions used by the various groups. Comprehensive and systematic studies on the influence of the implantation conditions on ion-induced CS splitting are still missing.

By using H implantation, Jalaguier et al. (164) and Tong et al. (165) were the first to demonstrate the transfer of three-inch GaAs and InP thin layers onto oxidized Si substrates. Following these pioneering works, research groups at SOITEC/LETI, UCLA, UCSD, Caltech, and MPI-Halle have reported the splitting of InP and GaAs thin layers with a diameter up to four inches by using H and/or He implantation (68, 164–171). The typical optimal implantation fluences range from 5×10^{16} to 1×10^{17} atom cm^{-2} for ion energies in the 50–150-keV range. **Figures 9** and **10** display electron microscopy images of InP and GaAs thin layers transferred from four-inch wafers onto Si(001) substrates. As mentioned above, the stress generated by thermal mismatch remains a serious obstacle to achieving high-quality bonding and splitting of large-diameter wafers. Coating CS substrates with a thin SOG layer before bonding to thermally oxidized Si(001) handle wafers leads to a very high surface energy, which helps to alleviate thermal stress–induced debonding (167, 171). However, the advantage of SOG is diminished (if not canceled) by the fact that the fabricated heterostructures cannot sustain high temperature in subsequent epitaxy and device fabrication because of outgassing issues associated with the SOG material. Appropriately annealed SiO_2 grown by PECVD would be the suitable interlayer for high-temperature processing of InP-on-Si and GaAs-on-Si substrates. However, due to the relatively lower surface energy in the case of SiO_2-to-Si hydrophilic bonding, thermal stress problems will have greater impact. Here the bonded wafers can debond and even break upon the thermal annealing necessary to activate splitting. In some cases, bonding and annealing under a compressive force are efficient in compensating for interfacial stress (168). In general, the surface of the transferred layers is usually rough (see, e.g., **Figure 9*c***). Obviously, any growth on such substrates will lead to poor-quality device structures. Therefore, it is necessary to remove the residual defective layer. For this reason, the as-split layers should be subject to a chemomechanical polishing (CMP) process to obtain an epi-ready surface (**Figure 9*d***).

The fabrication of large-diameter InP-on-Si and GaAs-on-Si heterostructures offers additional flexibility in the design and realization of bulk-quality heterogeneous devices. HEMTs

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

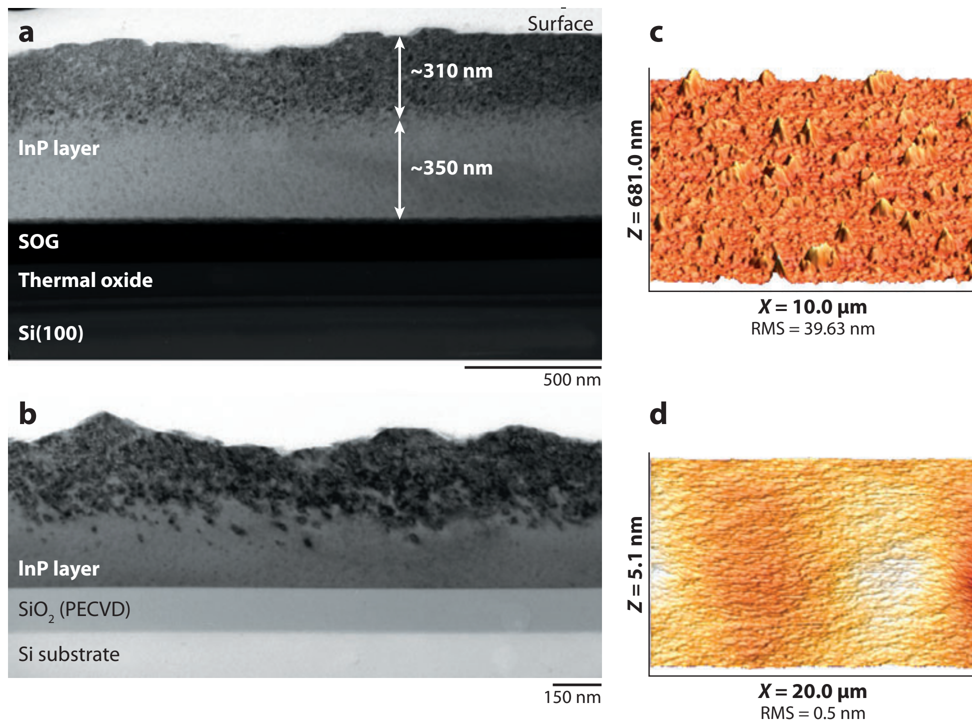

Figure 9

(*a*) Cross-sectional TEM image of a InP thin layer transferred from a four-inch wafer onto a Si(001) substrate using a SOG interlayer. Panel *a* adapted from Reference 168. (*b*) Cross-sectional TEM image of a InP thin layer transferred from a four-inch wafer onto a Si(001) substrate using a SiO_2 interlayer deposited by PECVD. (*c*) AFM image of the surface of the transferred layer. (*d*) AFM image of the surface of the transferred layer after a chemomechanical polishing (CMP) process. The corresponding root mean square (RMS) roughness is indicated on each AFM image.

were recently demonstrated on InP-on-Si and GaAs-on-Si heterostructures obtained by the ion-cut approach (166). Similarly, Atwater and coworkers (70) demonstrated high-efficiency InGaAs solar cells on Si realized by InP layer transfer. Another example is the successful integration of InP/InGaAs/InP *p-i-n* photodiodes on Si (32). In addition to InP and GaAs, layer transfer of SiGe alloys onto Si wafers was also demonstrated and exploited in the fabrication of strained SOI wafers with diameters of up to 300 mm (172).

APPLICATION TO BULK GaN

The ability to transfer several layers from a single donor wafer is of interest not only for the sake of bulk-quality heterostructures, which are frequently unattainable by direct epitaxy, but also to save and reduce materials cost. This particularly applies to very expensive substrates such as cadmium zinc telluride (173) and bulk GaN (fs-GaN) (109). Bulk-type GaN wafers of high crystalline quality are usually obtained by hydride vapor-phase epitaxy growth of thick GaN layers on sapphire substrates and subsequent separation from these substrates (174). These low-defect-density bulk GaN wafers are commercially available with a two-inch diameter [progress was recently achieved in the preparation of three-inch wafers (175)] and are used in the fabrication of

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

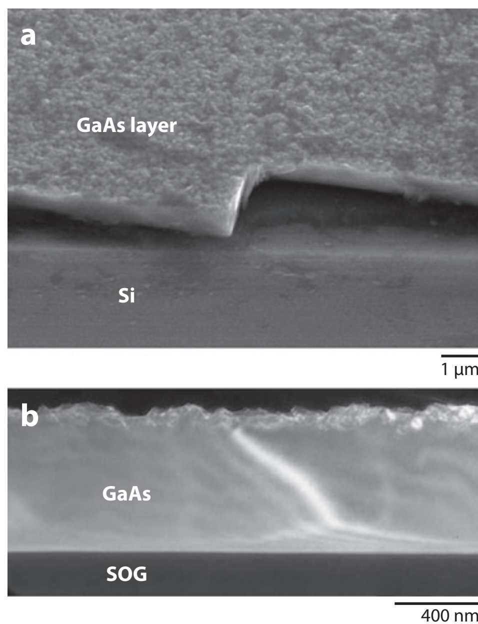

Figure 10

(*a*) Scanning electron microscopy and (*b*) cross-sectional TEM images of a GaAs thin layer transferred onto a Si substrate using the ion-cut process. Adapted from Reference 171.

blue laser diodes. Beyond these current applications, the availability of these fs-GaN substrates can potentially impact the fabrication of other devices such as power devices and ultrahigh-brightness light-emitting diodes. However, the current cost of fs-GaN wafers remains too high to allow for a large-scale production of these new devices. Therefore, to compete with alternative technologies (e.g., SiC), a decrease in bulk GaN cost is needed. Aiming at this goal, researchers of Arrowhead Research Corporation claimed in 2007 to have achieved the splitting of up to 10 layers from one-inch bulk GaN wafers by using the ion-cut process. Recently, we explored the possibility of applying this process to transfer thin GaN layers from the more technologically relevant two-inch bulk GaN donor wafers onto sapphire wafers (109). Here we describe some of the engineering aspects as well as our current understanding of the underlying physics of H ion cutting of GaN.

Engineering Issues

The major challenge in applying the ion-cut process to cleave bulk GaN has to do with the material morphology. As shown in **Figure 11**, commercially available wafers suffer from surface roughness, long-range waviness, and a significant bow. The ensemble of these surface imperfections and flatness deviations can limit the bonding quality or even prevent spontaneous bonding and, consequently, the application of the ion-cut process. To circumvent some of these difficulties, a SiO_2 cap layer can be deposited onto the GaN wafers. In addition to the fact that the SiO_2 layer can be easily polished, leading to smooth surfaces, the SiO_2/sapphire interface exhibits a fairly high bonding energy following annealing below 200°C (176). Moreover, the bonded interface shows high thermal stability after annealing up to 1050°C—the temperature used in the growth of GaN-based devices (**Figure 12**). To prevent undesired outgassing from the PECVD oxide layer during subsequent heat treatments of the bonded wafer pairs, it is important that the GaN wafers

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

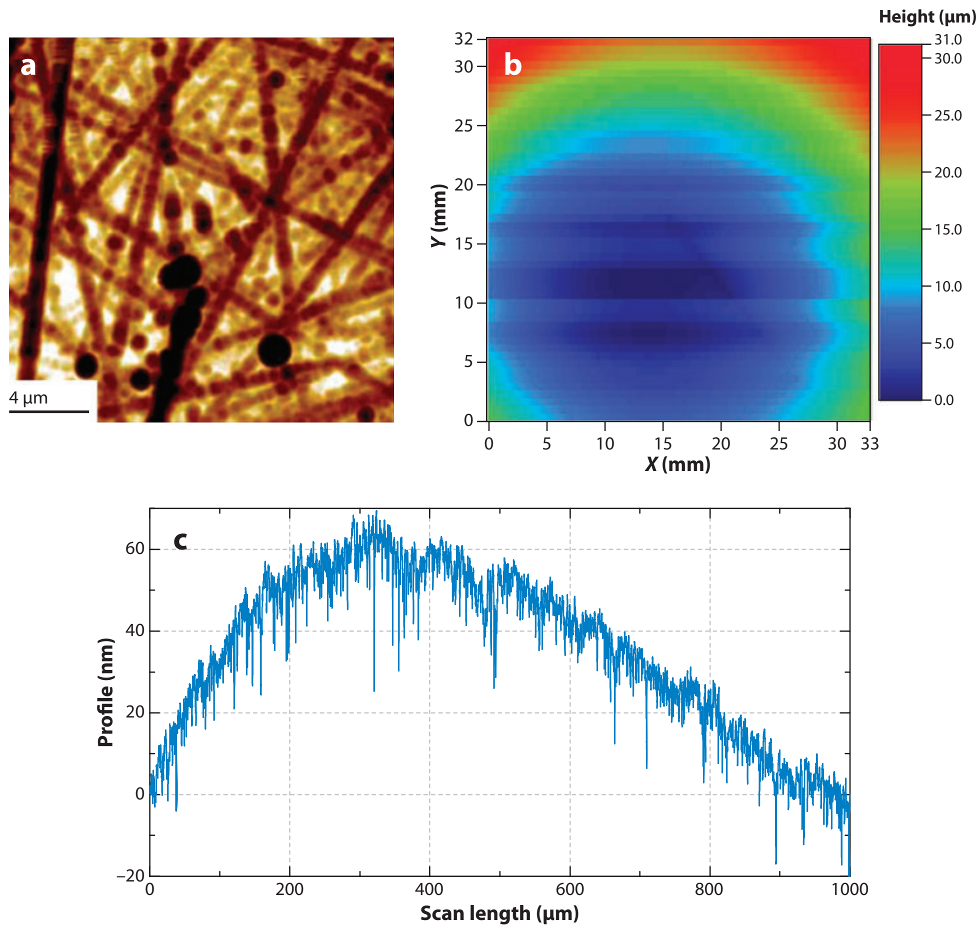

Figure 11

Morphological properties of commercially available two-inch freestanding GaN (fs-GaN). (*a*) A 20 µm × 20 µm AFM image of a N-face GaN surface. Typical RMS roughness ranges from 15 to 50 nm per 20 × 20 µm^2. (*b*) High-lateral-resolution measurement of the short-range surface waviness. (*c*) Two-dimensional map of surface profiles of a fs-GaN wafer.

be annealed at high temperature after SiO_2 layer deposition (109, 110). Oxide-deposited wafers are subsequently mirror polished via a CMP process. The CMP-finished surface RMS roughness is typically in the order of 0.2 nm per 20 × 20 µm^2 (**Figure 13*a***), ensuring the short-range flatness required for wafer bonding.

Oxide deposition and polishing can alleviate roughness as well as long-range waviness but hardly affect the bow, which increases further after ion implantation with the ion-cut optimal fluence of 2.6×10^{17} H cm^{-2} at 50 keV, as indicated in **Figure 13*b***. The origin of this postimplantation bowing of bulk GaN wafers is the volume increase and the resulting stress generated by implantation damage on the implanted side of the wafer. Unfortunately, the observed postimplantation bow is too high to allow any contacting of the wafers to be bonded. Indeed, the bonding experiments on as-implanted wafers show that the gap between the two surfaces is too large to permit even van der Waals forces to come into play to initiate the bonding process (168). Simple examination

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

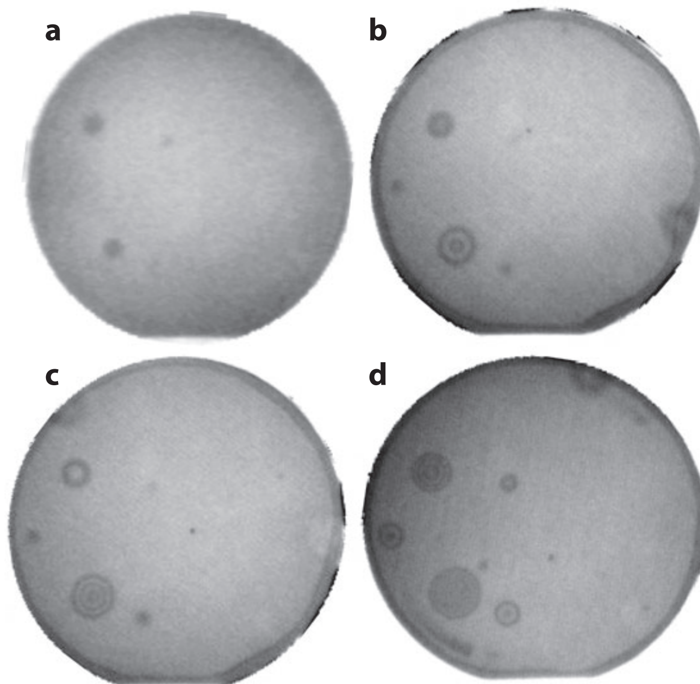

Figure 12

Infrared images of a bonded SiO_2/sapphire interface (*a*) immediately after room temperature bonding, (*b*) after annealing at 200°C for 24 h, (*c*) after annealing at 700°C for 2 h, and (*d*) after annealing at 1050°C for 2 h.

of Stoney's modified equation suggests that bow enhancement can be limited for thicker wafers (109). Under typical ion-cut conditions, the bow enhancement reaches ∼40 μm for 300-μm-thick fs-GaN. The increase in the thickness of a fs-GaN donor wafer by a factor n could reduce the bow enhancement by a factor n^2. However, the use of thick wafers to overcome the bow issue may lead to other difficulties in achieving good wafer bonding due to the relatively limited elastic deformation of thick substrates. Nevertheless, this process is worth testing, at least from a fundamental standpoint. Recently, double-sided implantation, under the same experimental conditions, was found to be effective in reducing the final bow (109). Moreover, a slightly deeper implantation at the back side can bring the bow to below its initial value in the virgin wafer, as shown in **Figure 13*b***. On the basis of this approach, bonding of two-inch H-implanted bulk GaN wafers to a sapphire wafer was accomplished (**Figure 14**).

The above-described method of wafer bow manipulation by stress adjustment at the back side of the implanted GaN leads to fairly flat H-implanted two-inch GaN wafers, making possible bonding to handle wafers. In spite of this achievement, complete transfer of two-inch-thin GaN layers from a fs-GaN wafer has not yet been demonstrated. One of the major problems in this regard is the partial or total debonding of GaN/sapphire pairs upon annealing at temperatures above 300°C. This observation is attributed to thermally induced interfacial stress, which can be reduced by performing the initial bonding at relatively high temperatures (177).

Because the main motivation behind the use of ion cutting is to reduce the cost of bulk-quality GaN layers, the second implantation needed to adjust the bow is an additional step that increases the cost of the ion-cut process. However, the second (back-side) implantation can, at

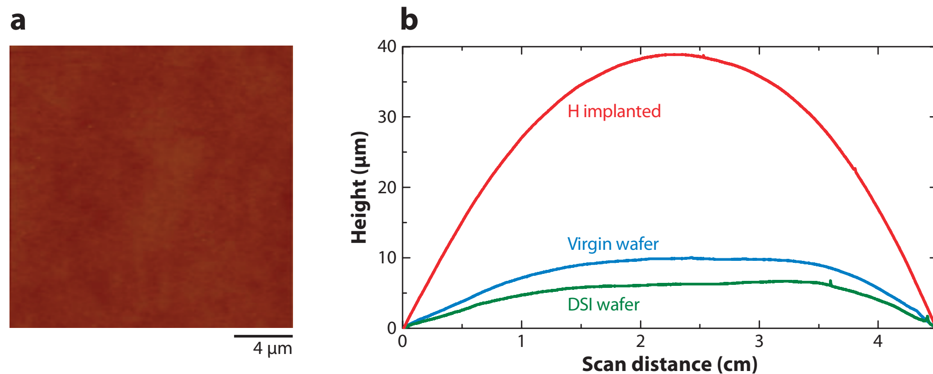

Figure 13

(*a*) A 20 μm × 20 μm AFM image of a N-face GaN surface after SiO_2 deposition by PECVD and after CMP processes. (*b*) Bow measurements on a two-inch bulk GaN wafer before implantation (virgin), after H implantation, and after double-sided implantation (DSI). The back-side implantation was performed with the same fluence but was approximately 50 nm deeper compared with the first implantation.

least in principle, be used not only to avoid excessive implantation-induced bow but also for the transfer of a second GaN layer. Indeed, the Ga face is also implanted at the optimal fluence, and therefore the bonding of both sides of fs-GaN wafers to two sapphire handle wafers can lead to the simultaneous transfer of two thin GaN layers by ion cutting (**Figure 15**). If required, the Ga-face heterostructure can be flipped to obtain a N-face layer, needed for epitaxial growth, by an additional bonding step and the subsequent release from the initial handle wafer.

Current Understanding of Basic Mechanisms

The need for a very high H ion fluence is one of the most striking differences between GaN and other CSs (and also Si) in which a fluence of a few 10^{16} H^+ cm^{-2} is sufficient to induce layer transfer. Supported by studies of damage buildup in GaN implanted with different ions (such as C, Si, or Au) (178), several authors have postulated that the high critical fluence has to be attributed

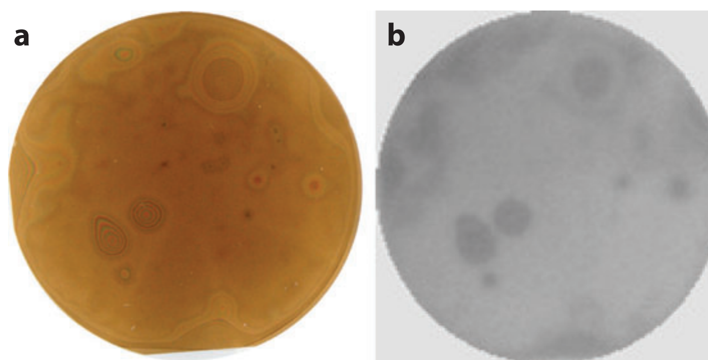

Figure 14

(*a*) Optical and (*b*) infrared micrographs of H-implanted ∼300-μm-thick fs-GaN bonded to a two-inch sapphire wafer. Due to radiation damage, fs-GaN wafers can change in appearance from transparent to golden brown after H implantation (109).

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

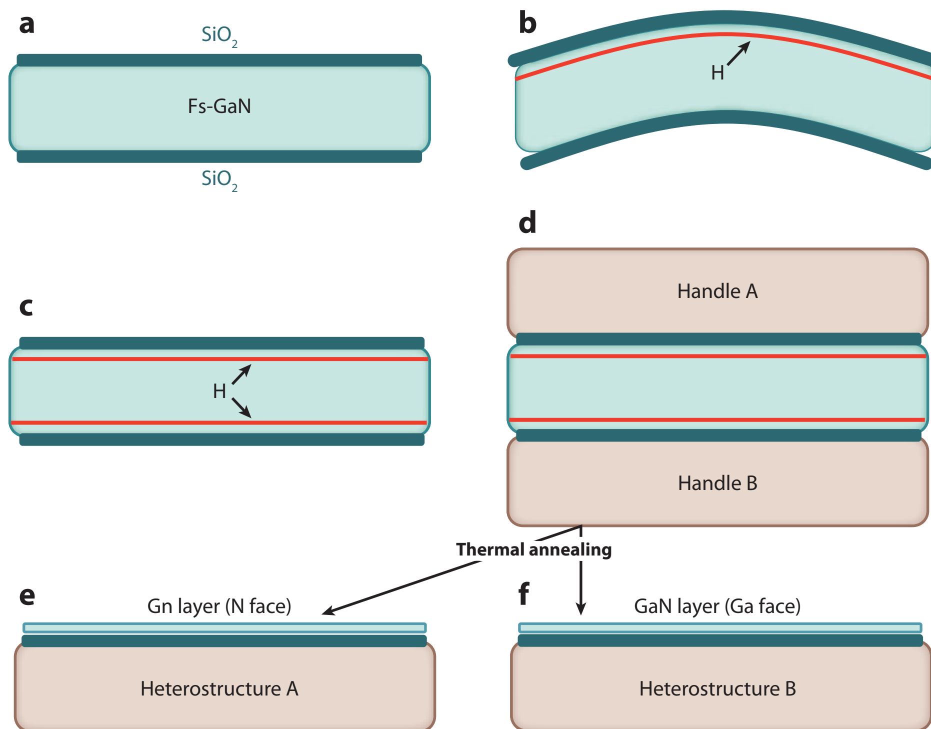

Figure 15

Schematic illustration of the double-sided bonding and splitting processes. (*a*) Deposition and polishing of an oxide on both sides of the wafer. (*b*) N-face H-implantation. (*c*) Ga-face H implantation and wafer bow reduction. (*d*) Direct bonding to two handle wafers. (*e*) Thermal annealing and simultaneous transfer of two thin films from a fs-GaN wafer. Two different handle wafers can be used, leading to different heterostructures in a one-step process.

to very efficient dynamic annealing of point defects in GaN (179–182). This explanation stands in sharp contrast to the blistering behavior of GaN implanted with H at low temperatures. Indeed, no change in the critical fluence is observed when implantation is carried out at liquid-nitrogen temperature, at which the dynamic annealing of point defects should be significantly reduced (179). In contrast, low-temperature implantation increases the required thermal budget for blistering and splitting, indicating that a larger accumulation of defects makes blistering even harder to trigger (179). Therefore, it appears that the high critical fluence can hardly be attributed to pronounced dynamic annihilation of implantation-induced point defects. The extrapolation of data obtained with other ions to the H case can be fraught with uncertainty. It is more likely that one has to consider the chemical reactivity of H and the stabilizing effect of dangling-bond passivation in addressing defect dynamic annealing and damage buildup in H-implanted semiconductors (183). Alternatively, the intrinsic mechanical properties as well as the nature of H-induced defects may be critical in determining the fluence of H ions needed to cleave GaN. Another peculiarity of GaN is the absence of the otherwise common synergistic effect on successive implantations with He and H ions in both orders, which is efficient in reducing the critical fluence and thermal budget in other semiconductors (see, e.g., References 170 and 184 and references therein). Intriguingly, we observed that the implantation of He alone requires the same critical fluence as H. Also, the critical fluence does not vary when highly *p*-doped GaN is used instead of undoped GaN. In

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

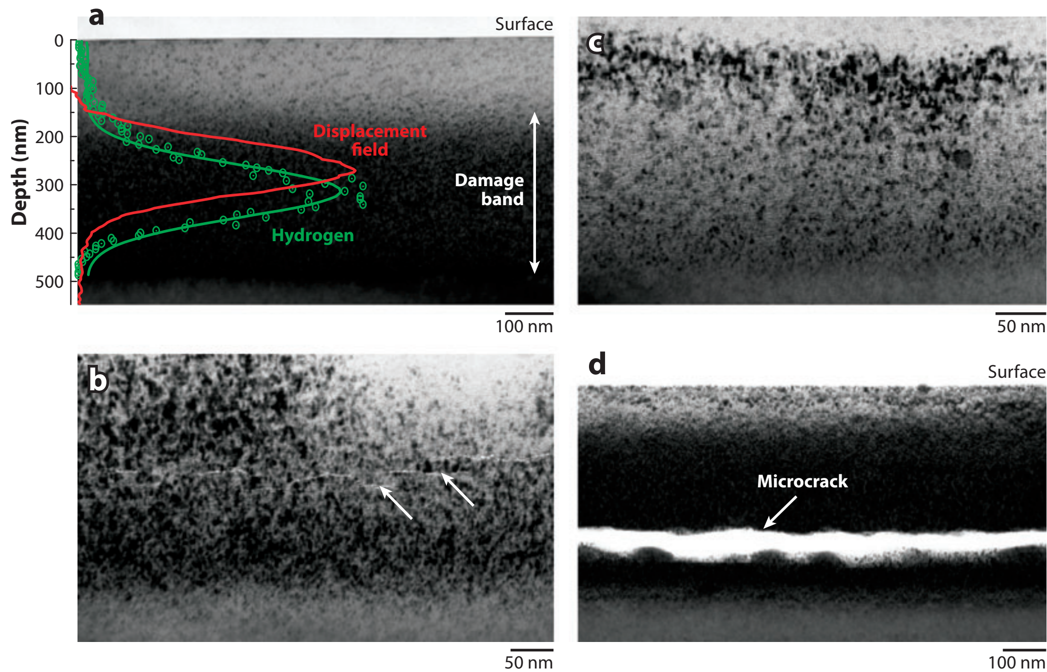

Figure 16

Cross-sectional TEM images of H-implanted GaN at a fluence of 2.6×10^{17} cm^{-2} at 50 keV (*a*) immediately after implantation, (*b*) after annealing at 450°C, (*c*) at 500°C (the *arrows* indicate nanoscopic cracks), and (*d*) at 600°C for 5 min. H and displacement profiles as measured by elastic recoil detection and ion channeling are superposed onto the as-implanted image. Adapted from Reference 139.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

contrast, for Si the critical fluence decreases drastically for highly *p*-doped substrates (161). These observations suggest that the phenomenon of ion-induced layer transfer may be fundamentally different in GaN as compared with other well-studied semiconductors.

On the basis of a variety of experimental techniques, **Figures 16** and **17** depict the nature of the microstructure produced after implantation of undoped GaN under ion-cut conditions and its thermal behavior. During the implantation of energetic H ions into GaN, several physical and chemical processes take place, leading to a variety of damage-related structures, including point defects in both sublattices, H-defect complexes, point defect clusters, and free H. H ion implantation induces a broad damage band extending over a 300-nm-thick layer starting at approximately 200 nm below the surface (**Figure 16*a***). No extended defects are observed at the implanted fluence. Weinstein et al. (185) published a first attempt to experimentally identify H-defect complexes in H-implanted GaN. They found that the infrared absorption spectrum of as-implanted GaN displays two main vibrational bands centered at 3139.5 and 3023.1 cm^{-1} (as measured at liquid-He temperature). These modes were attributed to H trapped in N dangling-bond defects near a Ga vacancy (V_{Ga}). The band at the highest frequency was attributed to a V_{Ga}-H_4 mode, whereas the band at the lowest frequency was associated with V_{Ga}-H_n complexes, which contained fewer H atoms (i.e., $n \leq 3$). However, the data obtained by Weinstein et al. cannot be extended directly to the condition of ion-cut process because the fluence implanted in their case is approximately two orders of magnitude lower than the critical fluence of H exfoliation of GaN. Indeed, the infrared spectrum of H-implanted GaN (**Figure 17*a***) indicates that a large fraction of H is trapped in higher-frequency modes $k > 3140$ cm^{-1} (beyond the V_{Ga}-H_4 frequency), which can

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

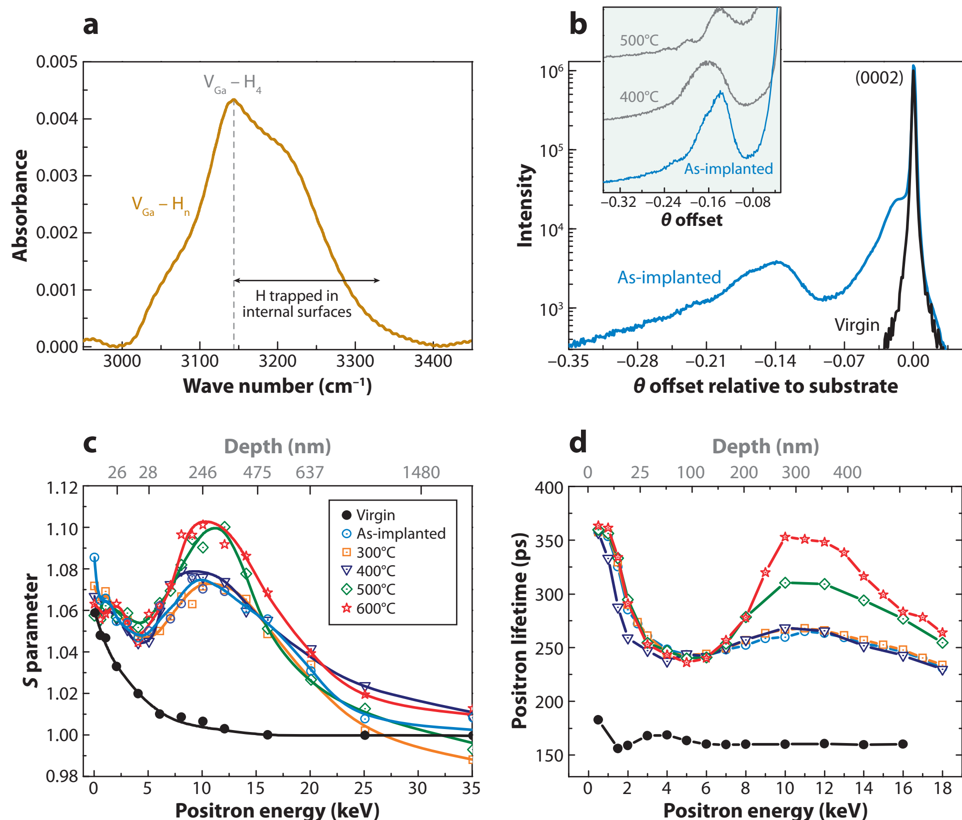

Figure 17

(*a*) Vibrational spectrum measured at room temperature of H-implanted GaN at a fluence of 2.6 × 10^{17} cm^{-2}. (*b*) High-resolution X-ray diffraction $\theta/2\theta$ scans of (0002) GaN before and after H implantation. The inset shows the evolution of damage-induced strain after annealing at 400°C and at 500°C (the intensities are given in linear scale). (*c*) Thermoevolution of the normalized *S* parameter of H-implanted GaN samples as a function of incident positron energy. For comparison, the spectrum recorded from bulk GaN is also shown. (*d*) The evolution of the average positron lifetime, measured by pulsed low-energy positron lifetime spectroscopy, as a function of the positron energy for the virgin, as-implanted, and annealed GaN samples. The decomposition of lifetime spectra indicates that the observed increase in the average lifetime above 450°C is associated with the formation of positronium in subnanoscopic cracks, which are embryos of extended internal surfaces.

be tentatively attributed to N-H stretch modes at the internal surfaces of implantation-induced nanobubbles (139). No Ga-H (or V_N-H)-related mode was detected. High-resolution X-ray data (**Figure 17*b***) and positron annihilation data (**Figure 17*c***) demonstrate, immediately after implantation, the generation of a significant out-of-plane tensile strain that is detectable as a broadening at the left side of the (0002) GaN diffraction peak and the presence of open-volume defects in the damage band. From lifetime positron annihilation spectroscopy (**Figure 17*d***), these open defects are likely divacancies and Ga vacancy clusters chemically stabilized by H (186). By following the thermal evolution of these complexes, one can deduce a mechanistic picture of H ion cutting of GaN: Annealing up to ∼400–450°C induces an enhancement in the internal strain (**Figure 17*b***) without any increase in the density of open-volume defects (**Figures 16*b*** and **17*c***). This implies that vacancy clusters and voids needed to prepare the ground for the splitting assemble during the

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

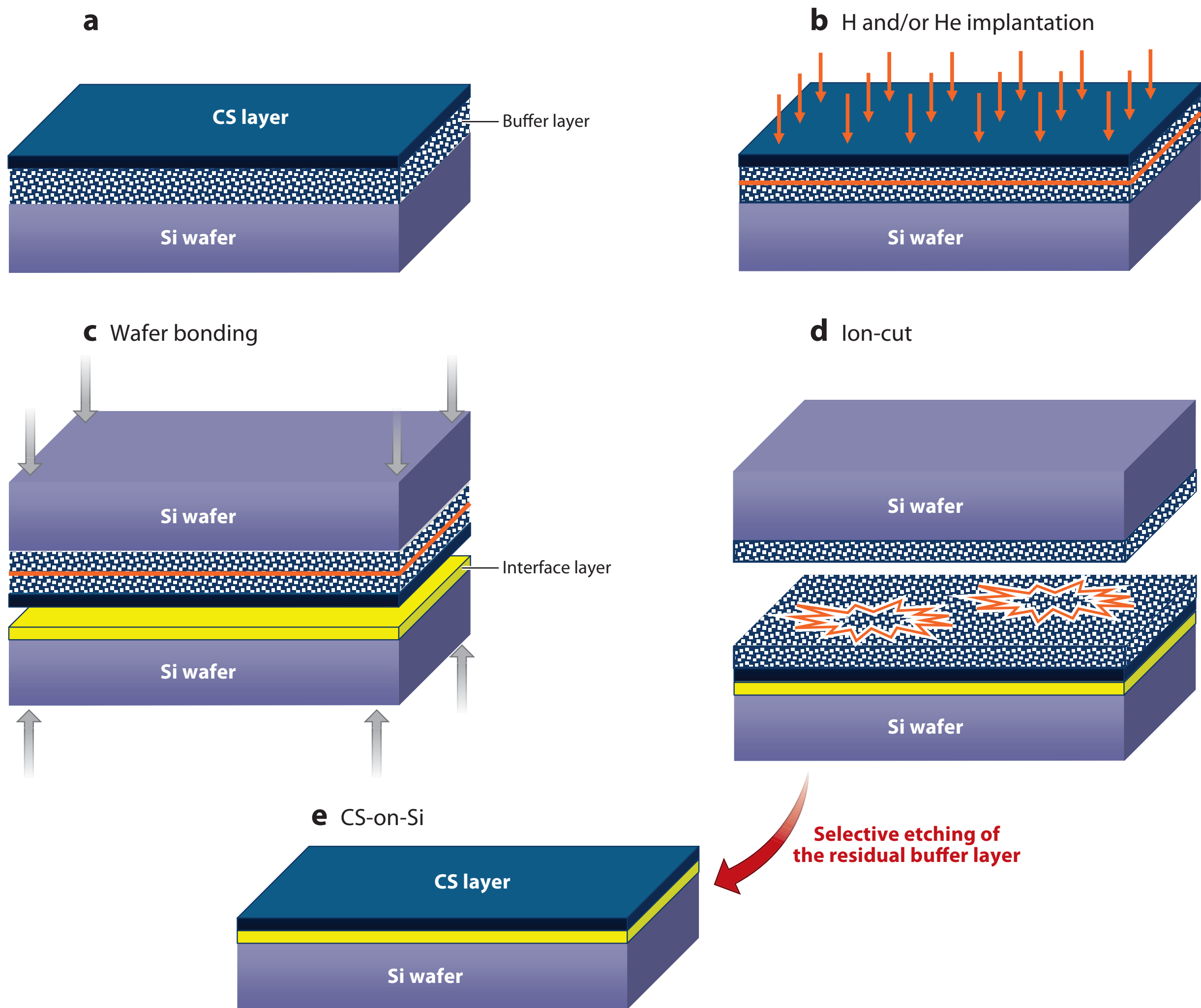

Figure 18

Schematic illustration of the integration on the wafer scale of a CS layer. (*a*) Growth of a high-quality CS layer on a metamorphic composite buffer layer deposited on a Si wafer. (*b*) Ion implantation. The implantation energy can be chosen such that the splitting zone takes place in the buffer layer. (*c*) Wafer bonding to a handle Si wafer. SiO_2 can be used as the interfacial layer. (*d*) Activation of the splitting process. (*e*) Elimination of the residual buffer layer by selective etching. This process flow is analogous to the process used in the fabrication of strained SOI wafers.

implantation process and remain relatively stable upon annealing below the critical temperature. This high thermal stability of open-volume defects may be one of the reasons behind the need for the exceedingly high ion fluence in GaN ion cutting. In contrast, for Si, for which the critical fluence is much lower, an important growth in void-like defects was reported in the temperature range preceding the splitting (155). Annealing above the ∼400–450°C temperature range leads to the formation of nanoscopic cracks parallel to the surface (**Figure 16*c***), inducing a partial relaxation of the internal strain (**Figure 17*b***). At higher temperatures, these cracks evolve into extended internal surfaces, leading to the splitting of the top thin layer (**Figure 16*d***). Therefore, it is

reasonable to conclude that the ion-cut process originates from the relaxation of the buildup of the internal strain induced by the evolution of the implantation damage with increasing temperature. However, the exact nature of the factors responsible for this strain enhancement remains an open challenge. The formation and trapping of H_2 molecules as well as the formation of interstitial clusters are possible candidates, but their detection in GaN remains elusive.

CONCLUSION

The capacity to tailor CSs and to integrate them onto foreign substrates can lead to superior or novel functionalities. In this review we provide a brief description of different approaches to realize these promising heterodevices. We show that the ion-cut process offers additional flexibility in the design and fabrication of CS-based heterostructures, which can be used in a wide range of technologies. However, for a heterogeneous integration process to be economically viable and attractive for CMOS applications, it must offer the possibility of integrating CSs onto large Si wafers. It is currently not possible to make large-diameter CSs, which can be a serious restriction in the application of CS ion cutting at the industrial level. It is, however, premature to exclude ion cutting in the heterointegration of wafers involving large diameters (300 mm and above). An attractive option, illustrated in **Figure 18**, may be a hybrid CS heterointegration process combining the progress in heteroepitaxy on Si and ion cutting in analogy to the process currently used in the fabrication of large-diameter strained SOI wafers. Here the highly defective interfacial layer can be eliminated, and only the top layer containing high-crystalline-quality CS film or quantum well structures is preserved and transferred to a desired host wafer using the appropriate dielectric interlayer.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

SUMMARY POINTS

1. Direct epitaxy, wafer bonding, or both can be used to integrate CSs onto foreign materials. The physical and structural properties of the CS material and the host substrate as well as the subsequent treatments of the obtained heterostructures and the targeted applications are the most influential factors in the choice of the appropriate heterointegration approach.
2. If bulk quality is needed, thin-layer transfer using the ion-cut process provides an approach to realizing certain heterodevices and flexible devices frequently unattainable by direct epitaxy.
3. The ion-cut process consists of wafer bonding and subsurface defect engineering using light ion implantation. The stability of the bonded interface is very critical to both the thin-layer transfer process and subsequent processing of the obtained heterodevice. Therefore, a successful layer transfer and a reliable heterostructure would require a meticulous conditioning of surfaces to be bonded as well as the use of a compatible interlayer.
4. In spite of thermal mismatch–related difficulties, InP-on-Si and GaAs-on-Si heterostructures with a diameter up to four inches were demonstrated by using the ion-cut process.
5. Progress has been made toward the splitting of two-inch bulk GaN by using the ion-cut process. The major concern of radiation damage–induced bow enhancement is alleviated by stress engineering at the back side of the donor wafer.

FUTURE ISSUES

1. It is of interest to explore the application of thin-layer transfer by the ion-cut process in other CS materials of technological relevance such as InSb and bulk AlN.
2. To develop a quantitative and predictive model of the ion-cut process, theoretical and experimental investigations of H/He-defect interactions in CSs as well as systematic studies of the influence of the implantation conditions on the splitting behavior are needed. These studies are vital for better control of the ion-cut technology.
3. Stress induced by thermal mismatch will remain a serious obstacle for the application of the ion-cut process to transfer large-diameter CS thin layers. To date, researchers and engineers have relied on the use of dielectric interlayers (e.g., SiO_2) for relatively low temperature bonding of CS wafers to Si wafers despite the limited bonding energy achieved via hydrophilic bonding. Alternatively, progress in molecular design and synthesis can provide serious solutions to achieve the high bonding energy, low thermal budget, and high thermal stability needed for the fabrication and processing of CS-based heterodevices. For instance, appropriately designed monolayers can be used as interfacial layers to bond CS wafers to different host materials. Such developments can also impact other areas involving wafer bonding such as three-dimensional integration and microelectromechanical systems.
4. The advantages of atomic layer deposition (ALD) should be exploited in CS thin-layer transfer. ALD can be used to grow atomically smooth and highly uniform interfacial dielectric films on surfaces to be bonded. This way, effort and time needed for CMP can be saved. Moreover, this technique also permits the deposition of high-quality Al_2O_3 layers suitable for CS-based electronic heterodevices.
5. A wide variety of freestanding semiconductor nanomembranes can be fabricated using the ion-cut process. These interesting nanomaterials can be obtained by releasing the transferred ultrathin layers from their host substrates. This ability to produce nanomembranes provides a rich playground for designing flexible devices and for exploring the fundamental properties of different semiconductors on the nanoscale.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

DISCLOSURE STATEMENT

The authors are not aware of any affiliations, memberships, funding, or financial holdings that might be perceived as affecting the objectivity of this review.

ACKNOWLEDGMENTS

Heartfelt thanks are extended to our colleagues and collaborators: R. Scholz, I. Hopfe, S. Senz, M. Alexe, S. Christiansen, M. Reiche, M. Chicoine, R. Krause-Rehberg, A. Avramescu, U. Strauss, and Y. Chabal. O.M. is thankful to T. Yonehara for stimulating discussions. This work was supported in part by the German Federal Ministry of Education and Research BMBF (contract number 01BU0624: CrysGaN).

LITERATURE CITED

1. Arthur WB. 2009. *The Nature of Technology: What It Is and How It Evolves*. New York: Free Press

2. Deboeck J, Zou G, Vanrossum M, Borghs G. 1991. Mesa release and deposition used for GaAs-on-Si MESFET fabrication. *Electron. Lett.* 27:22–23
3. Shieh CL, Chi JY, Armiento CA, Haugsjaa PO, Negri A, et al. 1991. 1.3 μm InGaAsP ridge waveguide laser on GaAs and silicon substrates by thin-film transfer. *Electron. Lett.* 27:850–51
4. Camperiginestet C, Kim YW, Jokerst NM, Allen MG, Brooke MA. 1992. Vertical electrical interconnection of compound semiconductor thin-film devices to underlying silicon circuitry. *IEEE Photon. Tech. Lett.* 4:1003–6
5. Ersen A, Schnitzer I, Yablonovitch E, Gmitter T. 1993. Direct bonding of GaAs films on silicon circuits by epitaxial liftoff. *Electron. Lett.* 36:1731–39
6. Service RS. 2009. Is silicon's reign nearing its end? *Science* 323:1000–2
7. Steckl AJ, Park JH, Zavada JM. 2007. Prospects for rare earth doped GaN lasers on Si. *Mater. Today* 10:20–27
8. Fang AW, Park H, Kuo Y-H, Jones R, Cohen O, et al. 2007. Hybrid silicon evanescent devices. *Mater. Today* 10:28–35
9. Roelkens G, Van Campenhout J, Brouckaert J, Van Thourhout D, Baets R, et al. 2007. III-V/Si photonics by die-to-wafer bonding. *Mater. Today* 10:36–43
10. Ghani T, Armstrong M, Auth C, Bost M, Charvat P, et al. 2003. A 90 nm high-volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors. *Int. Electron Devices Meet. Tech. Dig.* 2003:978–80
11. **Heyns M, Tsai W. 2009. Ultimate scaling of CMOS logic devices with Ge and III-V materials. *MRS Bull.* 34:485–88**

11. Addresses technical issues at the device level currently faced in the processing of CS-based CMOS.

12. Hudait MK, Dewey G, Datta S, Fastenau JM, Kavalieros J, et al. 2007. Heterogeneous integration of enhancement mode $In_{0.7}Ga_{0.3}As$ quantum well transistor on silicon substrate using thin ($\leq 2\,\mu m$) composite buffer architecture for high-speed and low-voltage (0.5V) logic applications. *Int. Electron Devices Meet.* 2007:625–28
13. **Herrick KJ, Kazior TE, Laroche J, Liu AWK, Lubyshev D, et al. 2008. Engineering substrates for 3D integration of III-V CMOS. *ECS Trans.* 16:227–34**

13. The first demonstration of an InP-based heterojunction bipolar transistor on Si wafer using the ion-cut process.

14. Fitzgerald EA, Bulsara MT, Bai Y, Cheng C, Liu WK, et al. 2009. Monolithic III-V/Si integration. *ECS Trans.* 19:345–50
15. Razeghi M, Defour M, Blondeau R, Omnes F, Maurel P, et al. 1988. First CW operation of a $Ga_{0.25}In_{0.75}As_{0.5}P_{0.5}$-InP laser on a silicon substrate. *Appl. Phys. Lett.* 53:2389–90
16. Bidnyk S, Little BD, Cho YH, Krasinski J, Song JJ, et al. 1998. Laser action in GaN pyramids grown on (111) silicon by selective lateral overgrowth. *Appl. Phys. Lett.* 73:2242–44
17. Yablonskii GP, Lutsenko EV, Pavlovskii VN, Zubialevich VZ, Gurskii AL, et al. 2002. Luminescence and stimulated emission from GaN on silicon substrates heterostructures. *Phys. Status Solid. A* 192:54–59
18. Mi Z, Bhattacharya P, Yang J, Pipe KP. 2005. Room-temperature self-organised $In_{0.5}Ga_{0.5}As$ quantum dot laser on silicon. *Electron. Lett.* 41:742–43
19. Seo S-W, Cho S-Y, Jokerst NM. 2005. A thin-film laser, polymer waveguide, and thin-film photodetector cointegrated onto a silicon substrate. *IEEE Photon. Technol. Lett.* 17:2197–99
20. Park JH, Steckl AJ. 2005. Demonstration of a visible laser on silicon using Eu-doped GaN thin films. *J. Appl. Phys.* 98:056108
21. Kwon O, Boeckl JJ, Lee ML, Pitera AJ, Fitzgerald EA, et al. 2006. Monolithic integration of AlGaInP laser diodes on SiGe/Si substrates by molecular beam epitaxy. *J. Appl. Phys.* 100:013103
22. Fang AW, Park H, Cohen O, Jones R, Paniccia MJ, et al. 2006. Electrically pumped hybrid AlGaInAs-silicon evanescent laser. *Opt. Express* 14:9203–10
23. Liang D, Fang AW, Oakley DC, Napoleone A, Chapman DC, et al. 2008. 150 mm InP-to-silicon direct wafer bonding for silicon photonic integrated circuits. *ECS Trans.* 16:235–41
24. Patterson PR, Elliott K, Li JC, Royter Y, Hussain T. 2008. Integration of compound semiconductor devices and CMOS (CoSMOS) with die to wafer bonding. *ECS Trans.* 16:221–25
25. Chang-Chien P, Gutierrez-Aitken A, Sandhu R, Hennig K, Scott D, et al. 2008. 3D wafer-scale integration for RF and digital applications. *ECS Trans.* 16:243–49
26. **Ahn J-H, Kim H-S, Lee KJ, Jeon S, Kang SJ, et al. 2006. Heterogeneous three-dimensional electronics by use of printed semiconductor nanomaterials. *Science* 314:1754–57**

26. Presents an ambitious heterointegration process using elastomeric stamp–based direct transfer of nanodevices.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

27. Menard E, Bower CA, Carr J, Rogers JA. 2007. Transfer printed heterogeneous integrated circuits. *CS MANTECH Conf.*, Austin, Tex., pp. 203–5
28. Sun Y, Kim H-S, Menard E, Kim S, Adesida I, et al. 2006. Printed arrays of aligned GaAs wires for flexible transistors, diodes, and circuits on plastic substrates. *Small* 2:1330–34
29. Meitl MA, Zhu Z, Kumar V, Lee KJ, Feng X, et al. 2006. Transfer printing by kinetic control of adhesion to an elastomeric stamp. *Nat. Mater.* 5:33–38
30. Park SI, Xiong YJ, Kim RH, Elvikis P, Meitl M, et al. 2009. Printed assemblies of inorganic light-emitting diodes for deformable and semitransparent displays. *Science* 325:977–81
31. Kang Y, Mages P, Clawson AR, Lau SS, Lo YH, et al. 2001. Wafer-fused *p-i-n* InGaAs/Si photodiode with photogain. *Appl. Phys. Lett.* 79:970–72
32. Chen P, Chen WV, Yu PKL, Tang CW, Lau KM, et al. 2009. Effects of hydrogen implantation damage on the performance of InP/InGaAs/InP *p-i-n* photodiodes transferred on silicon. *Appl. Phys. Lett.* 94:012101
33. Bakkers EPAM, Borgström MT, Verheijen MA. 2007. Epitaxial growth of III-V nanowires on group IV substrates. *MRS Bull.* 32:117–22
34. Kasai S, Katagiri T, Takayanagi J, Kawase K, Ouchi T. 2009. Reduction of phonon resonant terahertz wave absorption in photoconductive switches using epitaxial layer transfer. *Appl. Phys. Lett.* 94:113505
35. Kasai S, Tanabashi A, Kajiki K, Itsuji T, Kurosaka R, et al. 2009. Micro strip line-based on-chip terahertz integrated devices for high sensitivity biosensors. *Appl. Phys. Express* 2:062401
36. Levinshtein ME, Rumyantsev SL, Shur MS, eds. 2001. *Properties of Advanced Semiconductor Materials*. New York: Wiley
37. Markoç H. 2008. *Handbook of Nitride Semiconductors and Devices*. Vol. 1: *Materials Properties*, *Physics and Growth*. Weinheim: Wiley-VCH
38. Levinshtein M, Rumyantsev S, Shur M, eds. 1996. *Handbook Series on Semiconductor Parameters*, Vol. 1. Singapore: World Sci.
39. Yao T, Hong S-K, eds. 2009. *Oxide and Nitride Semiconductors: Processing*, *Properties*, *and Applications*. Berlin: Springer
40. Faber KT, Malloy K, eds. 1992. *The Mechanical Properties of Semiconductors*. London: Academic
41. Oda O. 2007. *Compound Semiconductor Bulk Materials and Characterizations*. Singapore: World Sci.
42. Becke H, Hall R, White J. 1965. Gallium arsenide MOS transistors. *Solid-State Electron*. 8:813–18
43. Becke HW, White JP. 1967. Gallium arsenide FETs outperform conventional silicon MOS devices. *Electronics* 40:82–85
44. Mimura T, Fukuta M. 1980. Status of the GaAs metal-oxide-semiconductor technology. *IEEE Trans. Electron Devices* 27:1147–55
45. Yea PD. 2008. Main determinants for III–V metal-oxide-semiconductor field-effect transistors. *J. Vac. Sci. Technol. A* 26:697–704
46. Kobayashi T, Taira K, Nakamura F, Kawai H. 1989. Band lineup for a GaInP/GaAs heterojunction measured by a high-gain *Npn* heterojunction bipolar transistor grown by metalorganic chemical vapor deposition. *J. Appl. Phys.* 65:4898–4902
47. Schuppen A, Erben U, Gruhle A, Kibbel H, Schumacher H, et al. 1995. Enhanced SiGe heterojunction bipolar transistors with 160GHz-f_{max}. *Int. Electron Devices Meet.* 1995:743–46
48. Nguyen C, Liu T, Chen M, Sun H-C, Rensch D. 1995. AlInAs/GaInAs/InP double heterojunction bipolar transistor with a novel base-collector design for power applications. *Int. Electron Devices Meet.* 1995:799–802
49. Bhat R, Hong W-P, Caneau C, Koza MA, Nguyen C-K, et al. 1996. InP/GaAsSb/InP and InP/GaAsSb/InGaAsP double heterojunction bipolar transistors with a carbon-doped base grown by organometallic chemical vapor deposition. *Appl. Phys. Lett.* 68:985–87
50. Han J, Baca AG, Shul RJ, Willison CG, Zhang L, et al. 1999. Growth and fabrication of GaN/AlGaN heterojunction bipolar transistor. *Appl. Phys. Lett.* 74:2702–4
51. Yuan JS. 1999. *SiGe*, *GaAs*, *and InP Heterojunction Bipolar Transistors*. New York: Wiley
52. Khan MA, Bhattarai A, Kuznia JN, Olson DT. 1993. High electron mobility transistor based on a GaN-Al_xGa_{1-x}N heterojunction. *Appl. Phys. Lett.* 63:1214–15

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

53. Kim D-H, del Alamo J. 2007. Logic performance of 40nm InAs HEMTs. *Int. Electron Devices Meet.* 2007:629–32
54. Datta S, Ashley T, Brask J, Buckle L, Doczy M, et al. 2005. 85 nm gate length enhancement and depletion mode InSb quantum well transistors for ultra high speed and very low power digital logic applications. *Int. Electron Devices Meet.* 2005:783–86
55. Ashley T, Buckle L, Datta S, Emeny MT, Hayes DG, et al. 2007. Heterogeneous InSb quantum well transistors on silicon for ultra-high speed, low power logic applications. *Electron. Lett.* 43:777–79
56. Canham LT. 1990. Silicon quantum array fabrication by electrochemical chemical dissolution of wafers. *Appl. Phys. Lett.* 57:1046–48
57. Lehmann V, Gösele U. 1991. Porous silicon formation: a quantum wire effect. *Appl. Phys. Lett.* 58:656–58
58. Pavesi L. 2003. Will silicon be the photonic material of the third millenium? *J. Phys. Condens. Matter* 15:R1169–96
59. Boyraz O, Jalali B. 2004. Demonstration of a silicon Raman laser. *Opt. Express* 12:5269–73
60. Rong H, Liu A, Jones R, Cohen O, Hak D, et al. 2005. An all-silicon Raman laser. *Nature* 433:292–94
61. Rong H, Kuo Y-H, Xu S, Liu A, Jones R, et al. 2006. Monolithic integrated Raman silicon laser. *Opt. Exp.* 14:6705–12
62. Park H, Fang AW, Cohen O, Jones R, Paniccia MJ, et al. 2007. A hybrid AlGaInAs-silicon evanescent amplifier. *IEEE Photon. Technol. Lett.* 19:230–32
63. Park H, Kuo YH, Fang AW, Jones R, Cohen O, et al. 2007. Hybrid AlGaInAs-silicon evanescent preamplifier and photodetector. *Opt. Exp.* 5:13539–46
64. Tsybeskov L, Lockwood DJ. 2009. Silicon-germanium nanostructures for light emitters and on-chip optical interconnects. *Proc. IEEE* 97:1284–303
65. Wanlass WM, Ward JS, Emery KA, Al-Jassim MM, Jones KM, et al. 1996. $Ga_xIn_{1-x}As$ thermophotovoltaic converters. *Sol. Energy Mater. Sol. Cells* 41:405–17
66. Kurtz SR, Allerman AA, Jones ED, Gee JM, Banas JJ, et al. 1999. InGaAsN solar cells with 1.0 eV band gap, lattice matched to GaAs. *Appl. Phys. Lett.* 74:729–31
67. Dahal R, Pantha B, Li J, Lin JY, Jiang HX. 2009. InGaN/GaN multiple quantum well solar cells with long operating wavelengths. *Appl. Phys. Lett.* 94:063505
68. Fontcuberta i Morral A, Zahler JM, Atwater HA, Ahrenkiel SP, Wanlass MW. 2003. InGaAs/InP double heterostructures on InP/Si templates fabricated by wafer bonding and hydrogen-induced exfoliation. *Appl. Phys. Lett.* 83:5413–15
69. Tanabe K, Fontcuberta i Morral A, Atwater HA, Aiken DJ, Wanlass MW. 2006. Direct-bonded GaAs/InGaAs tandem solar cell. *Appl. Phys. Lett.* 89:102106
70. **Zahler JM, Ladous C, Pinnington T, Newman FD, Atwater HA. 2007. High efficiency InGaAs solar cells on Si by InP layer transfer. *Appl. Phys. Lett.* 91:012108**
71. Kang BS, Ren F, Wang L, Lofton C, Tan WHW, et al. 2005. Electrical detection of immobilized proteins with ungated AlGaN/GaN high-electron-mobility transistors. *Appl. Phys. Lett.* 87:023508
72. Kang BS, Pearton SJ, Chen JJ, Ren F, Johnson JW, et al. 2006. Electrical detection of deoxyribonucleic acid hybridization with AlGaN/GaN high electron mobility transistors. *Appl. Phys. Lett.* 89:122102
73. Kang BS, Wang HT, Ren F, Pearton SJ. 2008. Electrical detection of biomaterials using AlGaN/GaN high electron mobility transistors. *J. Appl. Phys.* 104:031101
74. Wolf SA, Awschalom DD, Buhrman RA, Daughton JM, von Molnár S, et al. 2001. Spintronics: a spin-based electronics vision for the future. *Science* 294:1488–95
75. De Boeck J, Van Roy W, Das J, Motsnyi V, Liu Z, et al. 2002. Technology and materials issues in semiconductor-based magnetoelectronics. *Semicond. Sci. Technol.* 17:342–54
76. Demeester P, Ackaert A, Coudenys G, Moerman I, Buydens L, et al. 1991. Relaxed lattice-mismatched growth of III-V semiconductors. *Prog. Cryst. Growth Charact. Mater.* 22:53–141
77. Akiyama M, Kawarada Y, Kaminishi K. 1984. Growth of single domain GaAs layer on (100)-oriented Si substrate by MOCVD. *Jpn. J. Appl. Phys.* 23:L843–45
78. Ueda T, Nishi S, Kawarada Y, Akiyama M, Kaminishi K. 1986. Effects of the substrate offset angle on the growth of GaAs on Si substrate. *Jpn. J. Appl. Phys.* 25:L789–91

70. The first demonstration of a high-efficiency CS-based photovoltaic cell on Si using the ion-cut process.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

79. Kim YH, Lee JY, Noh YG, Kim MD, Kwon YJ, et al. 2006. Effect of two-step growth on the heteroepitaxial growth of InSb thin film on Si (001) substrate: a transmission electron microscopy study. *Appl. Phys. Lett.* 89:031919
80. Tausch FW Jr, Lapierre AG III. 1965. A novel crystal growth phenomenon: single crystal GaAs overgrowth onto silicon dioxide. *J. Electrochem. Soc.* 112:706–9
81. McClelland RW, Bozler CO, Fan JCC. 1980. A technique for producing epitaxial films on reuseable substrates. *Appl. Phys. Lett.* 37:560–62
82. Shichijo M, Nakane R, Sugahara S, Takagi S. 2007. Fabrication of III-V on insulator structures on Si using microchannel epitaxy with a two-step growth technique. *Jpn. J. Appl. Phys.* 46:5930–34
83. Tanoto H, Yoon SF, Loke WK, Chen KP, Fitzgerald EA, et al. 2008. Heteroepitaxial growth of GaAs on (100) Ge/Si using migration enhanced epitaxy. *J. Appl. Phys.* 103:104901
84. Choi D, Kim E, McIntyre PC, Harris JS. 2008. Molecular-beam epitaxy growth of III-V semiconductors on Ge/Si for metal-oxide-semiconductor device fabrication. *Appl. Phys. Lett.* 92:203502
85. Nakaharai S, Tezuka T, Sugiyama N, Moriyama Y, Takagi S. 2003. Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique. *Appl. Phys. Lett.* 83:3516–18
86. Wagner RS, Ellis WC. 1964. Vapor-liquid-solid mechanism of single crystal growth. *Appl. Phys. Lett.* 4:89–90
87. Yazawa M, Koguchi M, Hiruma K. 1991. Heteroepitaxial ultrafine wire-like growth of InAs on GaAs substrates. *Appl. Phys. Lett.* 58:1080–82
88. Hiruma K, Yazawa M, Katsuyama T, Ogawa K, Haraguchi K. 1995. Growth and optical properties of nanometer-scale GaAs and InAs whiskers. *J. Appl. Phys.* 77:447–62
89. Martensson T, Svensson CPT, Wacaser BA, Larsson MW, Seifert W, et al. 2004. Epitaxial III-V nanowires on silicon. *Nano Lett.* 4:1987–90
90. Chuang LC, Moewe M, Chase C, Kobayashi NP, Chang-Hasnain C. 2007. Critical diameter for III-V nanowires grown on lattice-mismatched substrates. *Appl. Phys. Lett.* 90:043115
91. Yi SS, Girolami G, Amano J, Islam MS, Sharma S, et al. 2006. InP nanobridges epitaxially formed between two vertical Si surfaces by metal-catalyzed chemical vapor deposition. *Appl. Phys. Lett.* 89:133121
92. Gösele U, Tong QY. 1998. Semiconductor wafer bonding. *Annu. Rev. Mater. Sci.* 28:215–41
93. Tong QY, Gösele U. 1999. *Semiconductor Wafer Bonding: Science and Technology*. New York: Wiley
94. Haisma J, Spierings GACM. 2002. Contact bonding, including direct-bonding in a historical and recent context of materials science and technology, physics and chemistry: historical review in a broader scope and comparative outlook. *Mater. Sci. Eng. R* 37:1–60
95. Alexe M, Gösele U, eds. 2004. *Wafer Bonding: Applications and Technology*. Berlin: Springer-Verlag
96. Christiansen SH, Singh R, Gösele U. 2006. Wafer direct bonding: from advanced substrate engineering to future applications in micro/nanoelectronics. *Proc. IEEE* 94:1–46
97. Knechtel R. 2005. Glass frit bonding: an universal technology for wafer level encapsulation and packaging. *Microsyst. Technol.* 12:63–68
98. Niklaus F, Stemme G, Lu J-Q, Gutmann RJ. 2006. Adhesive wafer bonding. *J. Appl. Phys.* 99:031101
99. Wallis G, Daniel IP. 1969. Field assisted glass-metal sealing. *J. Appl. Phys.* 40:3946–49
100. Lehmann V, Mitani K, Stengl R, Mii T, Gösele U. 1989. Bubble-free wafer bonding of GaAs and InP on silicon in a microcleanroom. *Jpn. J. Appl. Phys.* 28:L2141–43
101. Yu SL, Mages P, Qiao D, Jia L, Yu PKL, et al. 2003. Photocurrent method for characterizing the interface of hydrophobically bonded Si wafers. *Appl. Phys. Lett.* 82:916–18
102. Fecioru AM. 2006. *Low temperature UHV bonding with laser precleaning*. PhD thesis. Martin-Luther-Univ. Halle-Wittenberg. 101 pp.
103. Kim MJ, Carpenter RW. 2003. Heterogeneous silicon integration by ultrahigh vacuum wafer bonding. *J. Electron. Mater.* 32:849–54
104. Pasquariello D, Camacho M, Ericsson F, Hjort K. 2001. Crystalline defects in InP-to-silicon direct wafer bonding. *Jpn. J. Appl. Phys.* 40:4837–44
105. Liang D, Bowers JE. 2008. Highly efficient vertical outgassing channels for low-temperature InP-to-silicon direct wafer bonding on the silicon-on-insulator substrate. *J. Vac. Sci. Technol. B* 26:1560–68
106. Tong QY, Gan Q, Hudson G, Fountain G, Enquist P. 2004. Low temperature InP/Si wafer bonding. *Appl. Phys. Lett.* 84:732–34

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

107. Alexe M, Dragoi V, Reiche M, Gösele U. 2000. Low temperature GaAs/Si direct wafer bonding. *Electron. Lett.* 36:677–78
108. Katsnelson A, Tokramov V, Yakimov M, Lamberti M, Oktyabrasky S. 2003. Hybrid integration of III-V optoelectronic devices on Si platform using BCB. *Mater. Res. Soc. Symp. Proc.* 741:123–28
109. Moutanabbir O, Senz S, Scholz R, Christiansen S, Avramescu A, et al. 2009. Stress adjustment and bonding of H-implanted 2-in. freestanding GaN wafer: the concept of double-sided splitting. *Electrochem. Solid-State Lett.* 14:H105–8
110. Tan CS, Fan A, Chen KN, Reif R. 2003. Low-temperature thermal oxide to plasma-enhanced chemical vapor deposition oxide wafer bonding for thin-layer transfer. *Appl. Phys. Lett.* 82:2649–51
111. Schmid-Fetzer R. 1995. Fundamentals of bonding by isothermal solidification for high temperature semiconductor applications. In *Design Fundamentals of High Temperature Composites, Intermetallics, and Metal-Ceramics Systems*, ed. Lin RY, Chang YA, Reddy RG, Liu CT, pp. 75–99. Warrendale, PA: Miner. Met. Mater. Soc.
112. Bickford J, Lau SS, Yu PKL. 2008. GaAs/Si metal waferbonding for heterogeneous integrated circuits. *Int. Conf. Solid-State Integrated-Circuit Technol., 9th, Beijing, China*, pp. 1180–83
113. Hung Q-A, Lu S-J, Tong Q-Y. 1989. Gallium arsenide on insulator by electrostatic bonding. *1989 IEEE SOS/SOI Technol. Conf.*, pp. 62–63
114. Liang D, Bowers JE. 2009. Photonic integration: Si or InP? *Electron. Lett.* 45:578–81
115. Wang CA, Shiau DA, Murphy PG, O'Brian PW, Huang RK, et al. 2004. Wafer bonding and epitaxial transfer of GaSb-based epitaxy to GaAs for monolithic interconnection of thermophotovoltaic devices. *J. Electron. Mater.* 33:213–17
116. Yonehara T, Sakaguchi K, Sato N. 1994. Epitaxial layer transfer by bond and etch back of porous Si. *Appl. Phys. Lett.* 64:2108–10
117. Yonehara T, Sakaguchi K. 2001. ELTRAN®; novel SOI wafer technology. *JSAP Int.* 4:10–16
118. Föll H, Carstensen J, Langa S, Christophersen M, Tiginyanu IM. 2003. Porous III–V compound semiconductors: formation, properties, and comparison to silicon. *Phys. Status Solid. A* 197:61–70
119. Buzynin AN, Buzynin YN, Belyaev AV, Luk'yanov AE, Rau EI. 2007. Growth and defects of GaAs and InGaAs films on porous GaAs substrates. *Thin Solid Films* 515:4445–49
120. Konagai M, Sugimoto M, Takahashi K. 1978. High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* 45:277–80
121. Yablonovitch E, Gmitter T, Harbison JP, Bhat R. 1987. Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* 51:2222–24
122. Bruel M. 1995. Silicon on-insulator material technology. *Electron. Lett.* 31:1201–2
123. Deguet C, Sanchez L, Akatsu T, Allibert F, Dechamp J, et al. 2006. Fabrication and characterization of 200 mm germanium-on-insulator (GeOI) substrates made from bulk germanium. *Electron. Lett.* 42:415–17
124. Chao Y-L, Scholz R, Reiche M, Gösele U, Woo JCS. 2006. Characteristics of germanium-on-insulators fabricated by wafer bonding and hydrogen-induced layer splitting. *Jpn. J. Appl. Phys.* 45:8665–70
125. Radu I, Szafraniak I, Scholz R, Alexe M, Gösele U. 2002. Ferroelectric oxide single-crystalline layers by wafer bonding and hydrogen/helium implantation. *Mater. Res. Soc. Symp. Proc.* 748:U1181–86
126. Ruglovsky JL, Park YB, Ryan CB, Atwater HA. 2002. Wafer bonding and layer transfer for thin film ferroelectrics. *Mater. Res. Soc. Symp. Proc.* 748:U11–16
127. Rabiei P, Gunter P. 2004. Optical and electro-optical properties of submicrometer lithium niobate slab waveguides prepared by crystal ion slicing and wafer bonding. *Appl. Phys. Lett.* 85:4603–5
128. Levy M, Osgood RM Jr, Liu R, Cross LE, Cargill GS III, et al. 1998. Fabrication of single-crystal lithium niobate films by crystal ion slicing. *Appl. Phys. Lett.* 73:2293–95
129. Levy M, Ghimire S, Bandyopadhyay AK, Hong YK, Moon K, et al. 2002. PZN-PT single-crystal thin film monomorph actuator. *Ferroelectr. Lett. Sect.* 29: 29–40
130. Chen F. 2009. Photonic guiding structures in lithium niobate crystals produced by energetic ion beams. *J. Appl. Phys.* 106:081101
131. Schrempel F, Gischkat T, Hartung H, Höche T, Kley E-B, et al. Ultrathin membranes in *x*-cut lithium niobate. *Opt. Lett.* 34:1426–28

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

132. Current MI, Liu W, Roth IS, Lamm AJ, En WG, et al. 2001. A plasma immersion implantation system for materials modification. *Surf. Coat. Technol.* 136:138–41
133. Terreault B. 2007. Hydrogen blistering of silicon: progress in fundamental understanding. *Phys. Status Solid. A* 204:2129–84
134. Zahler JM, Fontcuberta i Morral A, Griggs MJ, Atwater HA, Chabal YJ. 2007. Role of hydrogen in hydrogen-induced layer exfoliation of germanium. *Phys. Rev. B* 75:035309
135. David M-L, Pizzagalli L, Pailloux F, Barbot JF. 2009. Atomic scale structure of (001) hydrogen-induced platelets in germanium. *Phys. Rev. Lett.* 102:155504
136. Fontcuberta i Morral A, Zahler JM, Griggs MJ, Atwater HA, Chabal YJ. 2005. Spectroscopic studies of the mechanism for hydrogen-induced exfoliation of InP. *Phys. Rev. B* 72:085219
137. Chen P, Di Z, Nastasi M, Bruno E, Grimaldi MG, et al. 2008. Effects of hydrogen implantation temperature on InP surface blistering. *Appl. Phys. Lett.* 92:202107
138. Hayashi S, Goorsky M, Noori A, Bruno D. 2006 . Materials issues for the heterogeneous integration of III-V compounds. *J. Electrochem. Soc.* 153:G1011
139. Moutanabbir O, Scholz R, Senz S, Gösele U, Chicoine M, et al. 2008. Microstructural evolution in H ion induced splitting of freestanding GaN. *Appl. Phys. Lett.* 93:031916
140. Moutanabbir O, Chabal YJ, Chicoine M, Christiansen S, Krause-Rehberg R, et al. 2009. Mechanisms of ion-induced GaN thin layer splitting. *Nucl. Instrum. Methods B* 267:1264–68
141. Weng X, Ye W, Goldman RS, Mabon JC. 2004. Formation and blistering of GaAsN nanostructure layers. *J. Vac. Sci. Technol. B* 22:989–92
142. Collino RR, Dick BB, Naab F, Wang YQ, Thouless MD, et al. 2009. Blister formation in ion-implanted GaAs: role of diffusivity. *Appl. Phys. Lett.* 95:111912
143. Reutov VF, Ibragimov SS. 1983. Method for fabricating thin silicon wafers. *USSR Inventor's Certif. No. 1282757*
144. Henley F, Lamm A, Kang S, Liu Z, Tian L. 2008. Direct film transfer (DFT) technology for kerf-free silicon wafering. *Eur. Photovoltaic Solar Energy*, *23rd*, *Valencia*, 2BO.2.3
145. Primak W. 1963. Radiation-induced cavities and exfoliation. *J. Appl. Phys.* 34:3630–31
146. Cerofolini GF, Corni F, Frabboni S, Nobili C, Ottaviani G, et al. 2000. Hydrogen and helium bubbles in silicon. *Mater. Sci. Eng. R* 27:1–52
147. Weldon MK, Marsico VE, Chabal YJ, Agarwal A, Eaglesham DJ, et al. 1997. On the mechanism of the hydrogen-induced exfoliation of silicon. *J. Vac. Sci. Technol. B* 5:1065–1073
148. Weldon MK, Collot M, Chabal YJ, Venezia VC, Agarwal A, et al. 1998. Mechanism of silicon exfoliation induced by hydrogen/helium coimplantation. *Appl. Phys. Lett.* 73:3721–23
149. Chabal YJ, Weldon MK, Caudano Y, Stefanov BB, Raghavachari K. 1999. Spectroscopic studies of H-decorated interstitials and vacancies in thin-film silicon exfoliation. *Physica B* 273–274:152–63
150. Moutanabbir O, Terreault B. 2004. Raman-scattering elucidation of the giant isotope effect in hydrogen-ion blistering of silicon. *J. Chem. Phys.* 121:7973–86
151. Weber J, Fisher T, Hieckmann E, Hiller M, Lavrov EV. 2005. Properties of hydrogen induced voids in silicon. *J. Phys. Condens. Matter* 17:S2303–14
152. Moutanabbir O, Terreault B. 2005. Effects in synergistic blistering of silicon by coimplantation of H, D, and He ions. *Appl. Phys. Lett.* 86:051906
153. Nguyen P, Cayrefourcq I, Bourdelle KK, Boussagol A, Guiot E, et al. 2005. Mechanism of the Smart Cut™ layer transfer in silicon by hydrogen and helium coimplantation in the medium dose range. *J. Appl. Phys.* 97:083527
154. Höchbauer T, Misra A, Nastasi M, Mayer JW. 2002. Physical mechanisms behind the ion-cut in hydrogen implanted silicon. *J. Appl. Phys.* 92:2335–42
155. Moutanabbir O, Terreault B, Chicoine M, Schiettekatte F, Simpson PJ. 2007. Influence of isotopic substitution and He coimplantation on defect complexes and voids induced by H ions in silicon. *Phys. Rev. B* 75:075201
156. Di ZF, Wang YQ, Nastasi M, Shao L, Lee JK, et al. 2008. Evidence for ion irradiation induced dissociation and reconstruction of Si-H bonds in hydrogen-implanted silicon. *Appl. Phys. Lett.* 93:104103
157. Nastasi M, Höchbauer T, Lee J-K, Hirth JP, Ridgway M, et al. 2005. Nucleation and growth of platelets in hydrogen-ion-implanted silicon. *Appl. Phys. Lett.* 86:154102

133. State-of-the-art understanding of the underlying physics of H- and/or He-induced blistering and splitting of Si.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

158. Lee J-K, Lin Y, Jia QX, Höchbauer T, Jung HS, et al. 2006. Role of strain in the blistering of hydrogen-implanted silicon. *Appl. Phys. Lett.* 89:101901
159. Sousbie N, Capello N, Eymery J, Rieutord F, Lagahé C. 2006. X-ray scattering study of hydrogen implantation in silicon. *J. Appl. Phys.* 99:103509
160. Simpson PJ, Knights AP, Chicoine M, Dudeck K, Moutanabbir O, et al. 2008. Thermal evolution of defects produced by implantation of H, D and He in silicon. *Appl. Surf. Sci.* 255:63–67
161. Woo HJ, Choi HW, Kim GD, Kim JK, Kim KJ. 2009. Blistering/exfoliation kinetics of GaAs by hydrogen and helium implantations. *Surf. Coat. Technol.* 203:2370–74
162. Tong Q-Y, Gösele U. 1999. Wafer bonding and layer splitting for microsystems. *Adv. Mater.* 11:1409–25
163. Hayashi S, Bruno D, Goorsky MS. 2004. Temperature dependence of hydrogen-induced exfoliation of InP. *Appl. Phys. Lett.* 85:236–38
164. Jalaguier E, Aspar B, Pocas S, Michaud JF, Zussy M, et al. Transfer of 3 in GaAs film on silicon substrate by proton implantation process. *Electron. Lett.* 34:408–9
165. Tong Q-Y, Chao Y-L, Huang LJ, Gösele U. 1999. Low temperature InP layer transfer. *Electron. Lett.* 35:341–42
166. Di Cioccio L, Jalaguier E, Letertre F. 2005. III-V layer transfer onto silicon and applications. *Phys. Status Solid. A* 202:509–15
167. Singh R, Radu I, Scholz R, Himcinschi C, Gösele U, et al. 2006. Low temperature InP layer transfer onto Si by helium implantation and direct wafer bonding. *Semicond. Sci. Technol.* 21:1311–14
168. Moutanabbir O, Christiansen S, Senz S, Scholz R, Petzold M, et al. 2008. III-V and III-nitride engineered heterostructures: wafer bonding, ion slicing and more. *ECS Trans.* 16:251–62
169. Chen W, Chen P, Jing Y, Lau SS, Kuech TF, et al. 2007. Double-flip transfer of indium phosphide layers via adhesive wafer bonding and ion-cutting process. *Appl. Phys. Lett.* 90:052114
170. Joshi MB, Hayashi SL, Goorsky MS. 2008. Fabrication of transfer-enhanced semiconductor substrates by wafer bonding and hydrogen exfoliation techniques. *Electrochem. Solid State Lett.* 11:H236–39
171. Radu I. 2003. *Layer transfer of semiconductors and complex oxides by helium and/or hydrogen implantation and wafer bonding*. PhD thesis. Martin-Luther-Univ. Halle-Wittenberg. 99 pp.
172. Reiche M, Himcinschi C, Gösele U, Christiansen SH, Mantl S, et al. 2007. Strained silicon-on-insulator: fabrication and characterization. *ECS Trans.* 6:339–44
173. Bhattacharya RS, He P, Xu Y, Goorsky M. 2008. Ion beam layer separation of cadmium zinc telluride. *AIP Conf. Proc.* 1066:221–24
174. Park SS, Park I-W, Park SH. 2000. Free-standing GaN substrates by hydride vapor phase epitaxy. *Jpn. J. Appl. Phys.* 39:L1141–42
175. Yoshida T, Oshima Y, Eri T, Watanabe K, Shibata M, et al. 2008. Preparation of 3 inch freestanding GaN substrates by hydride vapor phase epitaxy with void-assisted separation. *Phys. Status Solid. A* 205:1053–55
176. Kopperschmidt P, Kästner G, Hesse D, Zakharov ND, Gösele U. 1997. High bond energy and thermomechanical stress in silicon and sapphire wafer bonding. *Appl. Phys. Lett.* 70:2972–74
177. Moutanabbir O, Gösele U. 2010. Bulk GaN ion cleaving. *J. Electron. Mater.* 39:482–88
178. Kucheyev SO, Williams JS, Pearson SJ. 2001. Ion implantation into GaN. *Mater. Sci. Eng. R* 33:51–108
179. Kucheyev SO, Williams JS, Jagadish C, Zou J, Li G. 2001. Blistering of H-implanted GaN. *J. Appl. Phys.* 91:3928–30
180. Radu I, Singh R, Scholz R, Gösele U, Christiansen S, et al. 2006. Formation of nanovoids in high-dose hydrogen implanted GaN. *Appl. Phys. Lett.* 89:031912
181. Singh R, Radu I, Gösele U, Christiansen SH. 2006. Investigation of hydrogen implantation induced blistering in GaN. *Phys. Status Solid. C* 3:1754–57
182. Woo HJ, Choi HW, Hong W, Park JH, Eum CH. 2009. Blistering kinetics of GaN by hydrogen implantation at high temperature. *Surf. Coat. Technol.* 203:2375–79
183. Moutanabbir O, Scholz R, Gösele U, Terreault B. 2009. Facile synthesis of highly stable *a*-Si by ion implantation of low-keV H isotopes. *Phys. Rev. B* 79:233202
184. Moutanabbir O, Terreault B. 2005. Effects in synergistic blistering of silicon by coimplantation of H, D, and He ions. *Appl. Phys. Lett.* 86:051906

166. Demonstration of HEMTs on four-inch GaAs and InP transferred onto Si wafers using the ion-cut process.

178. An in-depth study of radiation damage buildup in GaN implanted with different ions.

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

185. Weinstein MG, Song CY, Stavola M, Pearton SJ, Wilson RG, et al. 1998. Hydrogen-decorated lattice defects in proton implanted GaN. *Appl. Phys. Lett.* 72:1703–5
186. Moutanabbir O, Scholz R, Gösele U, Guittoum A, Jungmann M, et al. 2010. Experimental elucidation of vacancy complexes associated with hydrogen ion-induced splitting of bulk GaN. *Phys. Rev. B* 81:115205

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

Annual Review of Materials Research

Volume 40, 2010

Contents

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.

New Developments in Composite Materials

Biological Composites
John W.C. Dunlop and Peter Fratzl 1

On the Mechanistic Origins of Toughness in Bone
Maximilien E. Launey, Markus J. Buehler, and Robert O. Ritchie 25

Teeth: Among Nature's Most Durable Biocomposites
Brian R. Lawn, James J.-W. Lee, and Herzl Chai 55

Mechanical Principles of Biological Nanocomposites
Baohua Ji and Huajian Gao 77

Optimal Design of Heterogeneous Materials
S. Torquato 101

Physical Properties of Composites Near Percolation
C.-W. Nan, Y. Shen, and Jing Ma 131

Magnetoelectric Composites
G. Srinivasan 153

Self-Healing Polymers and Composites
B.J. Blaiszik, S.L.B. Kramer, S.C. Olugebefola, J.S. Moore, N.R. Sottos, and S.R. White 179

Steel-Based Composites: Driving Forces and Classifications
David Embury and Olivier Bouaziz 213

Metal Matrix Composites
Andreas Mortensen and Javier Llorca 243

Current Interest

The Indentation Size Effect: A Critical Examination of Experimental Observations and Mechanistic Interpretations
George M. Pharr, Erik G. Herbert, and Yanfei Gao 271

Plasticity in Confined Dimensions
Oliver Kraft, Patric A. Gruber, Reiner Mönig, and Daniel Weygand 293

Saturation of Fragmentation During Severe Plastic Deformation
R. Pippan, S. Scheriau, A. Taylor, M. Hafok, A. Hohenwarter, and A. Bachmaier 319

Ultrasonic Fabrication of Metallic Nanomaterials and Nanoalloys
Dmitry G. Shchukin, Darya Radziuk, and Helmuth Möhwald 345

Oxide Thermoelectric Materials: A Nanostructuring Approach
Kunihito Koumoto, Yifeng Wang, Ruizhi Zhang, Atsuko Kosuga, and Ryoji Funahashi 363

Inkjet Printing of Functional and Structural Materials: Fluid Property Requirements, Feature Stability, and Resolution
Brian Derby 395

Microfluidic Synthesis of Polymer and Inorganic Particulate Materials
Jai Il Park, Amir Saffari, Sandeep Kumar, Axel Günther, and Eugenia Kumacheva 415

Current-Activated, Pressure-Assisted Densification of Materials
J.E. Garay 445

Heterogeneous Integration of Compound Semiconductors
Oussama Moutanabbir and Ulrich Gösele 469

Electrochemically Driven Phase Transitions in Insertion Electrodes for Lithium-Ion Batteries: Examples in Lithium Metal Phosphate Olivines
Ming Tang, W. Craig Carter, and Yet-Ming Chiang 501

Electromigration and Thermomigration in Pb-Free Flip-Chip Solder Joints
Chih Chen, H.M. Tong, and K.N. Tu 531

The Structure of Grain Boundaries in Strontium Titanate: Theory, Simulation, and Electron Microscopy
Sebastian von Alfthan, Nicole A. Benedek, Lin Chen, Alvin Chua, David Cockayne, Karleen J. Dudeck, Christian Elsässer, Michael W. Finnis, Christoph T. Koch, Behnaz Rahmati, Manfred Rühle, Shao-Ju Shih, and Adrian P. Sutton 557

Index

Cumulative Index of Contributing Authors, Volumes 36–40 601

Errata

An online log of corrections to *Annual Review of Materials Research* articles may be found at http://matsci.annualreviews.org/errata.shtml

Annu. Rev. Mater. Res. 2010.40:469-500. Downloaded from arjournals.annualreviews.org
by WIB6417 - Max-Planck-Gesellschaft on 07/28/10. For personal use only.