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Comparison of the top-down and bottom-up approach to fabricate nanowire-based silicon/germanium heterostructures

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ABSTRACT

Silicon nanowires (NWs) and vertical nanowire-based Si/Ge heterostructures are expected to be building blocks for future devices, e.g. field-effect transistors or thermoelectric elements. In principle two approaches can be applied to synthesise these NWs: the 'bottom-up' and the 'top-down' approach. The most common method for the former is the vapour–liquid–solid (VLS) mechanism which can also be applied to grow NWs by molecular beam epitaxy (MBE). Although MBE allows a precise growth control under highly reproducible conditions, the general nature of the growth process via a eutectic droplet prevents the synthesis of heterostructures with sharp interfaces and high Ge concentrations. We compare the VLS NW growth with two different top-down methods: The first is a combination of colloidal lithography and metal-assisted wet chemical etching, which is an inexpensive and fast method and results in large arrays of homogenous Si NWs with adjustable diameters down to 50 nm. The second top-down method combines the growth of Si/Ge superlattices by MBE with electron beam lithography and reactive ion etching. Again, large and homogeneous arrays of NWs were created, this time with a diameter of 40 nm and the Si/Ge superlattice inside.

1. Introduction

Silicon nanowires (NWs) and vertical nanowire-based Si/Ge heterostructures are interesting research objects because of the possibility to produce and investigate quantum well and quantum dot structures. Furthermore, there are a lot of potential applications in industry as part of future electronic and optical devices, e.g. sensors or field-effect transistors [1–6]. Si/Ge NW heterostructures are also considered as components of thermoelectric devices [6–11]. While phonon scattering at the NW surface already reduces the thermal conductivity of Si NWs compared to bulk values, the thermoelectric figure of merit, *ZT*, can be improved even further by phonon scattering at sharp Si/Ge interfaces.

There are, however, still a lot of tasks that have to be accomplished. This includes the exact control of the NW position for future contacting as well as the positioning of the Ge layers, and also the challenge to produce sharp Si/Ge interfaces and high element concentrations within the Si and Ge part of the NWs.

In principle two approaches can be applied to synthesise Si NWs and Si/Ge NW heterostructures: i) the 'top-down' approach and ii) the 'bottom-up' approach. In the latter, the NWs are grown from the vapour phase via a catalyst, which is usually a liquid Au/Si alloy droplet in case of the popular vapour–liquid–solid (VLS) mechanism, but can also be a solid particle, with the name of the mechanism then changed to vapour–solid–solid (VSS) growth [12,13]. In contrast, the top-down approach is based on etching techniques, for instance metal-assisted wet chemical etching or reactive ion etching (RIE).

The VLS growth of Si NWs and other materials was already reported and investigated in the 1960s and 1970s [14–17]. Today, Si NWs are normally grown by chemical vapour deposition (CVD) [18–21]. Molecular beam epitaxy (MBE) is a deposition technique which can be used for both the VLS NW growth and also the fabrication of conventional Si/Ge heterostructures as part of the top-down approach. Since the deposition is done in an ultra high vacuum, crystal growth by MBE offers the advantage of a very clean environment and thus highly reproducible conditions. It also allows a precise control of the layer thickness and composition, but usually has far lower growth rates than other deposition techniques.

Nevertheless, because of the precise growth control, the diffusion-based VLS NW growth by MBE has been chosen as a representative bottom-up method and is compared with two different top-down methods concerning the structural properties of the NWs, especially focussing on the one hand on the control of the NW position and dimensions, and on the other hand on the position of the Ge layers, the achievable Ge concentrations and the abruptness of the Si/Ge interfaces. The first top-down method is a combination of colloidal lithography and metal-assisted wet chemical etching. The second top-down method combines the growth of Si/Ge superlattices by MBE with electron beam lithography (EBL) and RIE. The samples with the

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NWs were investigated by transmission electron microscopy (TEM) and high-resolution scanning electron microscopy (SEM). The Ge concentration was measured by many-beam TEM bright field imaging.

2. Bottom-up approach

It has been shown earlier that the VLS mechanism can also successfully be applied to grow Si NWs by MBE [22–25], as well as the possibility to incorporate Ge layers [25,26]. However, in contrast to CVD VLS Si NW growth, the Au/Si droplet does not act as a catalyst to crack precursor molecules. Instead, a gradient in the chemical potential leads to a net flux of impinging Si monomers towards the Au/Si droplet, especially the Au/Si droplet interface with the Si substrate. The total flux I of Si atoms can be written as $I = I_1 + I_2$. I_1 represents the monomers absorbed by the droplet through direct impingement, I_2 represents the net flux which is generated by the surface diffusion as mentioned before. Thus the difference in the length of the NW compared to the overgrown epilayer $\Delta l = l_{NW} - l_{epi}$ is fully determined by the net flux I_2.

2.1. Experimental details

The NWs were grown by MBE on <111>-oriented P doped 5″ Si wafers (n-type doping) which were cleaned by the conventional RCA procedure before their insertion into a Riber SIVA 45 MBE machine equipped with e-beam evaporators for Au, Si and Ge, as well as conventional effusion cells for doping with B or Sb. After an annealing process to remove the protective oxide layer, a 200 nm intrinsic Si buffer layer was grown at a substrate temperature $T = 550$ °C for better comparability of the experiments (Fig. 1a). Then, an Au thin film with a nominal thickness of 1.5 to 2 nm was deposited at $T = 525$ °C. The thickness of the film was measured *in situ* with an oscillating quartz crystal. Due to the high temperature of the wafer, an Au/Si eutectic alloy is formed immediately, as well as liquid Au/Si alloy droplets, which will later act as the catalysts for the NW growth (Fig. 1b). This step is immediately followed by a second Si deposition step at $T = 525$ °C (Fig. 1c). As a standard experiment, the nominal Si film thickness for this period was chosen to be 270 nm, which corresponds to a deposition time of 1.5 h at a growth rate of 0.05 nm/s. The Ge layers were either deposited interrupting the Si NW growth time (Fig. 1d) or afterwards (Fig. 1e) at growth rates of either 0.02 nm/s or 0.01 nm/s. The gold droplet on top of the NWs as well as the gold decoration at the side walls and on top of the epilayer can be removed in a solution containing 20 g KI and 5 g I_2 per 100 ml H_2O (Fig. 1f).

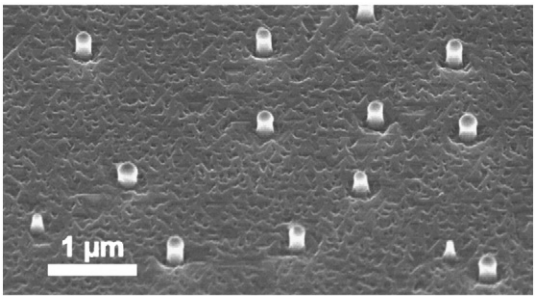

Fig. 2. SEM micrograph of a section of a Silicon wafer with Silicon nanowires. Theses nanowires grow perpendicular to the surface of the substrate. They are distributed randomly on the whole wafer and their diameters vary between 60 nm and 180 nm. The sample is tilted by 45°.

2.2. Results and discussion of the bottom-up approach

Fig. 2 shows a SEM micrograph image of a section of a 5″ wafer with VLS Si NWs grown by MBE. The NWs grow perpendicular to the wafer surface and are randomly distributed throughout the whole wafer. Their diameters vary between 60 nm and 180 nm. The NWs contain a Ge layer approximately in the middle of the visible part. This can be seen on the TEM micrograph in Fig. 3a. Fig. 3b shows the corresponding concentration profile. Since the length of the NW depends on its diameter and therefore on the diameter of the catalyst droplet [22], an exact positioning of the Ge layer can only be done when the diameter of the NW is adjusted before the growth. However, in any case where the catalyst is deposited as a film, only a diameter distribution is given. Nevertheless, if a medium growth rate of the NW is assumed for the average NW diameter, the position of the Ge layer can be adjusted with a high accuracy. In this case the total growth rate of the NW was 0.083 nm/s compared to 0.05 nm/s for the Si epilayer [27]. The Ge layer with a nominal epilayer thickness of 2.5 nm was placed between two deposition steps of 230 nm and 40 nm of

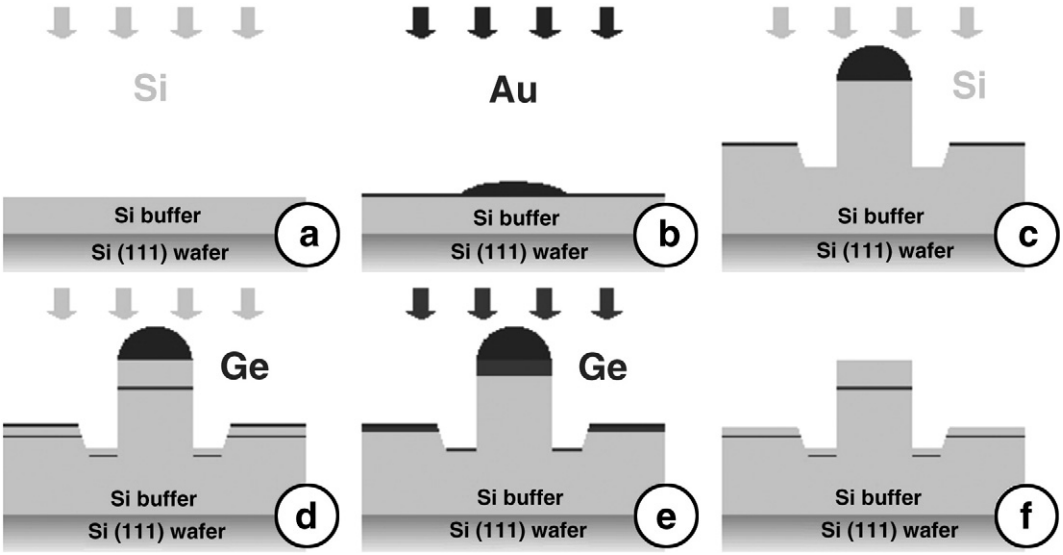

Fig. 1. Schematic diagram of the fabrication process of Silicon nanowires and Si/Ge heterostructure nanowires by molecular beam epitaxy. At first a Si buffer layer is grown (a). Then, an Au thin film with a nominal thickness of 1.5 to 2 nm is deposited (b). Liquid Au/Si alloy droplets are formed which will later act as the catalysts for the NW growth. This step is immediately followed by a second Si deposition step (c). Ge layers can be grown either interrupting the Si nanowire growth (d) or afterwards (e). The catalyst can be removed after the growth process (f).

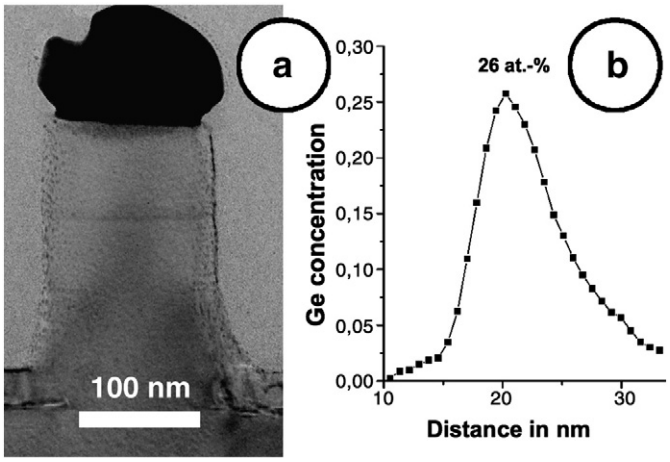

Fig. 3. (a) TEM micrograph of a Silicon nanowire. It contains a Germanium layer inside, roughly in the middle of the visible part. (b) Concentration profile measured along the growth direction. The maximum Germanium concentration found was 26 at.%. The FWHM of the profile is 7.5 nm.

Si. Thus the layer should have been 66.4 nm below the Au droplet. As measured from the TEM micrograph, the actual distance is approx. 68 nm.

Before the Ge deposition, the temperature was lowered from 525 °C to 360 °C, which is our standard growth temperature for pure Ge NWs on <111>-oriented Ge substrates. During the second Si deposition phase the temperature was increased back to 525 °C. Compared to results reported earlier [25], this simple yet effective step led to an increase in the Ge concentration by a factor of two up to 26 at.%. Although the nominal thickness of the Ge layer was increased from 1.5 nm to 2.5 nm, the FWHM could be decreased by approximately a factor of two from ≈ 15 nm to ≈ 8 nm. We expect the increase of the Ge concentration and the decrease of the FWHM to be a result of the reduction of the Si concentration within the eutectic droplet due to the lower temperature.

It has to be mentioned that it is not possible to synthesise these Si/Ge nanowire heterostructures at all if all parameters (growth rate and nominal epilayer thickness of 2.5 nm) are kept and the growth temperature remains constant at 525 °C. Any experiment that has been done under these conditions resulted in the dissolution of the

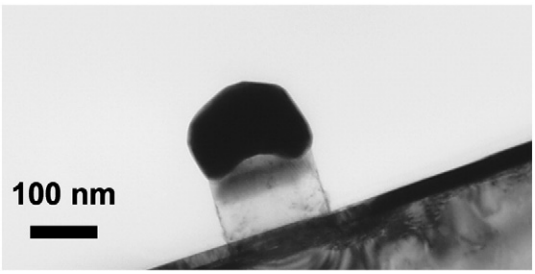

Fig. 5. TEM micrograph of a Germanium nanowire grown on top of a Silicon nanowire. The dark black spot on top is the Au catalyst, the middle part is a Ge rich $Si_{1-x}Ge_x$ alloy, and the bottom part is the Si nanowire.

NWs. This emphasizes our previous results which indicated a temperature dependent critical Ge concentration $x_c(T)$ leading to a stop of the NW growth. However, this effect of growth suppression due to Ge incorporation has up to now not been reported in the case of CVD Si NW growth.

Similar results concerning the thermal stability of Si/Ge heterostructures were obtained when we tried to continuously grow Ge NWs on Si NWs. Fig. 4 shows two SEM micrographs of MBE grown Si NWs where 20 nm Ge were deposited afterwards at 325 °C (left image) and 300 °C, respectively (right image). A lot of NWs have been destroyed in the first case, while all NWs remain intact at the lower temperature. A representative TEM micrograph of a NW from the second sample (Ge deposition at 300 °C) is seen in Fig. 5. The dark black spot on top is the Au catalyst, the middle part is a Ge rich $Si_{1-x}Ge_x$ alloy, and the bottom part is the Si NW. Since *in situ* TEM investigations during MBE growth are not possible at the present time, we cannot say if the Au catalyst was solid or liquid during the Ge deposition. Thus we cannot easily compare our results with those published by Kodambaka et al. who reported on the growth of Ge NWs below the eutectic temperature [13]. However, our growth temperature (300 °C) was below any known eutectic temperature of the ternary Au–Ge–Si system, which is assumed to have a minimum at 327 °C at a composition of 79 at.% Au, 7.5 at.% Ge and 13.5 at.% Si for the bulk material [28].

One of the open questions concerning the VLS growth mechanism was the potential inclusion of metal catalyst atoms, especially Au, into the growing NWs, because Au might act as a recombination centre and reduces the carrier lifetime in Si [29]. Recent advances in analytical methods like high-angle annular dark-field scanning transmission

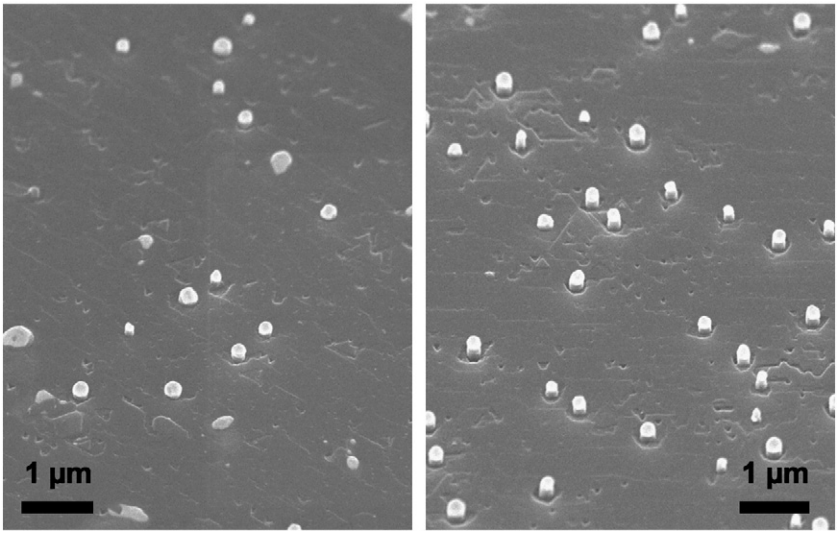

Fig. 4. SEM micrographs of samples where we tried to grow Germanium nanowires on top of Silicon nanowires. The Germanium was deposited at 325 °C (left image) and 300 °C, respectively (right image). A lot of nanowires have been destroyed in the first case, indicating that the temperature was too high for a continued growth. At the lower temperature all nanowires remain intact.

electron microscopy [30,31] and secondary ion mass spectroscopy at the nanoscale [32] enabled the detection of Au atoms within Si NWs. The maximum Au concentration was found to be $1.7\times10^{16}\mathrm{cm}^{-3}$ [32] and $5\times10^{17}\mathrm{cm}^{-3}$ [30]. These values are the same for MBE and CVD NW growth. Although for current Si NWs surface recombination controls the minority carrier transport and the influence of Au can be neglected, it has to be mentioned that this might change soon since an effective surface passivation and thus the reduction of surface states is one of many goals necessary for the successful implementation of NWs into devices.

2.3. Summary and conclusions on the bottom-up approach

We fabricated Si NWs with Ge layers inside and Ge NWs on top of Si NWs by MBE. The position of the Ge layers could be adjusted with high accuracy. However, although the Ge concentration for the layer could be improved by a reduction of the growth temperature compared to previous results, it remains low compared to conventional heterostructure layer growth by MBE. This result and also the results obtained from the continued growth of Ge NWs on Si NWs emphasize that, besides the diameter of the catalyst droplet, the growth temperature is one of the most critical process parameters. It not only greatly influences the Ge concentrations but also the stability of the NWs themselves. Furthermore, other groups have shown that catalyst atoms can be incorporated into the crystal lattices of the growing NWs as point defects, independent of the deposition technique. This questions the application potential of VLS grown Si NWs and also Si/Ge heterostructure NWs because these atoms might act as recombination centres.

3. Top-down approaches

3.1. Nanowire fabrication by colloidal lithography and metal-assisted wet chemical etching

Here, we demonstrate the fabrication of hexagonally-aligned vertical Si NWs, whose diameter, length and density can be controlled by localized chemical etching of Si through a metal-induced etching process. For this purpose, a method combining colloidal lithography, plasma etching and metal-assisted wet chemical etching was developed [33–36].

The working principle itself is based on a local oxidation and dissolution of the Si in a HF/H_2O_2 solution with a metal layer (like Ag, Au or Pt) acting as a catalyst [37–39]. This local dissolution of the oxidized Si and the simultaneous pitting at the same position causes the formation of pores in the Si substrate.

3.1.1. Experimental details

This process was adopted for a controlled fabrication of Si NWs. Fig. 6 shows the main experimental steps of this method. In a first step the Si substrate is pre-patterned by colloidal lithography. Self-ordered polymer spheres (obtained from microparticles GmbH as a 10 wt.% water solution) with diameters ranging from 200 nm to several microns were coated onto the Silicon surface by a mask transfer (panel 1). The monolayer fabrication is based on a self-assembling process of polymer spheres onto a water–air surface with the spheres forming a close-packed hexagonally arranged monolayer. Secondly, the diameter of the polymer spheres was modified by an O_2 plasma treatment at a flow rate of 400 sccm and a pressure of 0.06 mbar. The diameter and the centre-to-centre distance between the spheres are adjustable by the plasma etching time (panel b). Thirdly, a silver layer was deposited onto the modified polymer sphere mask by thermal evaporation. The thickness of the silver film amounts to 20 to 30 nm. Afterwards, the polymer sphere mask was removed by $CHCl_3$ in an ultrasonic bath, and as a result a metal layer with hexagonally ordered holes was obtained. This pre-structured substrate was soaked into an etching solution consisting of HF and H_2O_2 with concentrations of 4.6 and 0.44 M at room temperature. Only the areas which are not covered by silver remain unetched and form the Si NW array (panel e). The silver layer remains on the bottom of the Si NWs until it is eventually removed chemically by nitrohydrochloric acid (aqua regia) (panel f).

3.1.2. Results and discussion of metal-assisted etching

This top-down method allows the fabrication of well-ordered Si NWs with a hexagonal symmetry and adjustable diameters ranging from several microns down to 50 nm. The diameter of these NWs is

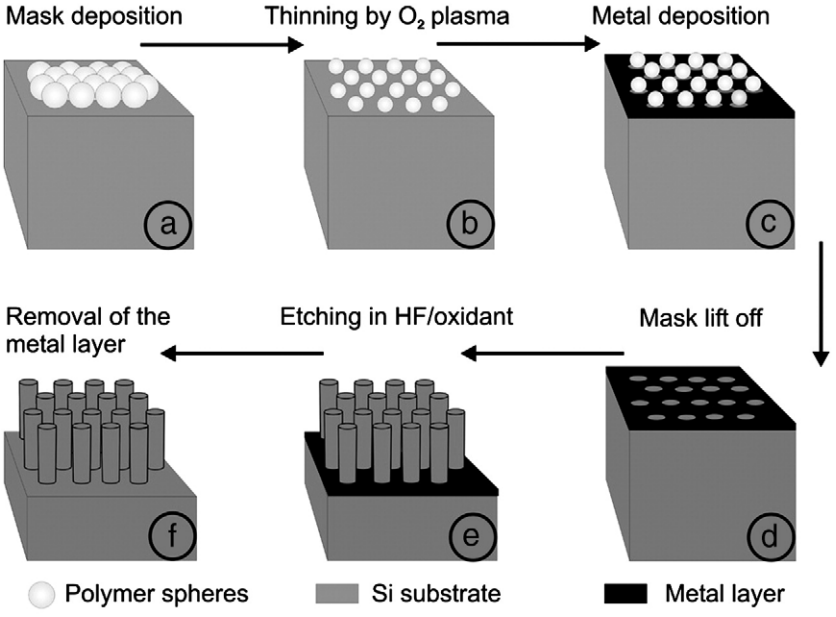

Fig. 6. Schematic diagram of the fabrication process of Si nanowires by metal-assisted wet chemical etching. The Silicon substrate (grey) is coated with a monolayer of hexagonally ordered close-packed polymer spheres (white) (panel a). O_2 plasma etching is carried out to form a non-close-packed polymer sphere mask, whereas the diameter of the spheres is controllable (panel b). A thin metal layer (black) is deposited onto the masked substrate (panel c). The polymer spheres are removed and a metal-hole mask remains (panel d). Etching of the pre-structured substrate in a HF/H_2O_2 solution to form Si nanowires (panel e). Removal of the metal layer (panel f).

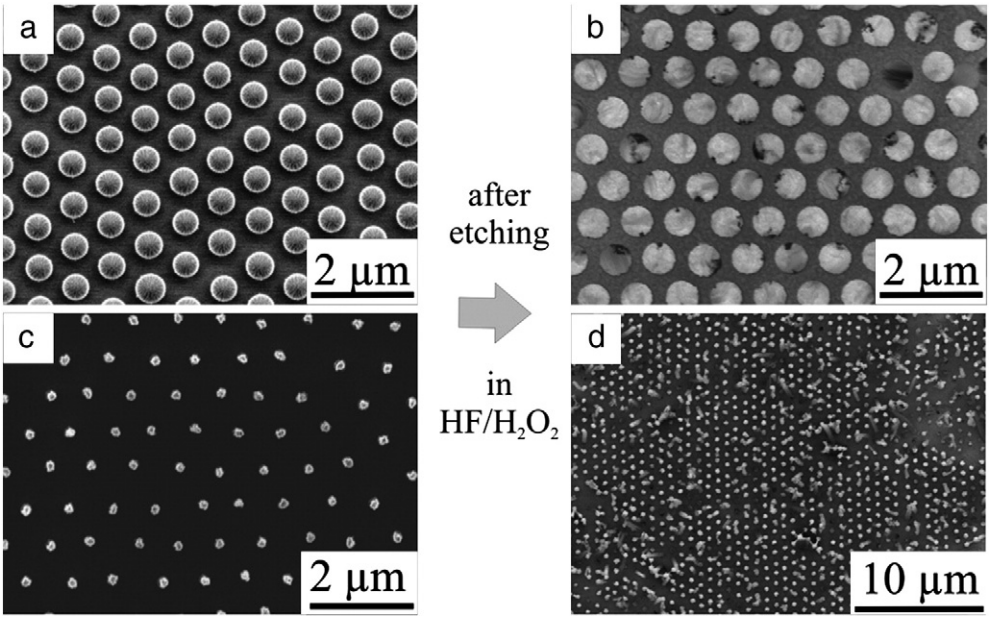

Fig. 7. Polymer sphere masks (nominal sphere diameter in both cases 780 nm) etched with different plasma etching times and the corresponding chemically etched Si nanowires: (a) setting a plasma etching time of 5 min the sphere diameter is reduced down to 530 nm and after the metal-assisted etching the etched nanowires also have a diameter of 530 nm (b). (c) After a plasma etching time of 20 min the spheres have a diameter of 220 nm and the etched nanowires, too (d).

determined by the diameter of the polymer spheres of the lithographic mask. Therefore the diameter of the NWs can be controlled by varying the etching time of the polymer spheres in oxygen plasma which can be seen in Fig. 7. The SEM micrographs show different plasma etched polymer sphere masks and the corresponding Si NWs obtained after the etching process. The nominal diameter of the polymer spheres is 780 nm. After a plasma etching treatment of 5 min (1) the spheres have a diameter of about 530 nm and after 20 min the diameter is reduced even further down to 220 nm. The etched Si NWs have the same diameter (see (b) and (d)) like the plasma etched spheres of the lithographic mask.

The length of the NWs can be varied by the etching time, while the density is determined by the original diameter of the polymer spheres. A high area density of about 10^{10} NWs/cm^2 can be obtained. The SEM images in Fig. 8 show Si NWs with a diameter of 1.8 µm (panel a) and 480 nm (panel b) which were fabricated over large (wafer-size) areas. All NWs have the same diameter and the same length which could be important for a later contacting of the NW arrays for electrical measurements.

3.1.3. Summary and conclusions on metal-assisted etching

Colloidal lithography combined with metal-assisted wet chemical etching is an inexpensive and fast method to produce large arrays of NWs with homogenous lengths and diameters and high area densities. However, the minimum diameter is limited to 50 nm. Therefore this method is not applicable for the investigation of quantum size effects. On the other hand, since Si/Ge structures can also be etched with this technique, it is interesting for the investigation of thermoelectric properties of Si/Ge heterostructure nanowires. A combination of this method with the growth of Si/Ge superlattice structures by MBE seems to be a promising approach to fabricate large arrays of Si/Ge heterostructure NWs for a potential application in thermoelectric devices.

3.2. Fabrication of vertical Si/Ge nanowire heterostructures by molecular beam epitaxy, electron beam lithography and reactive ion etching

For the second top-down method presented within this paper we combined the growth of a Si/Ge superlattice heterostructure by MBE

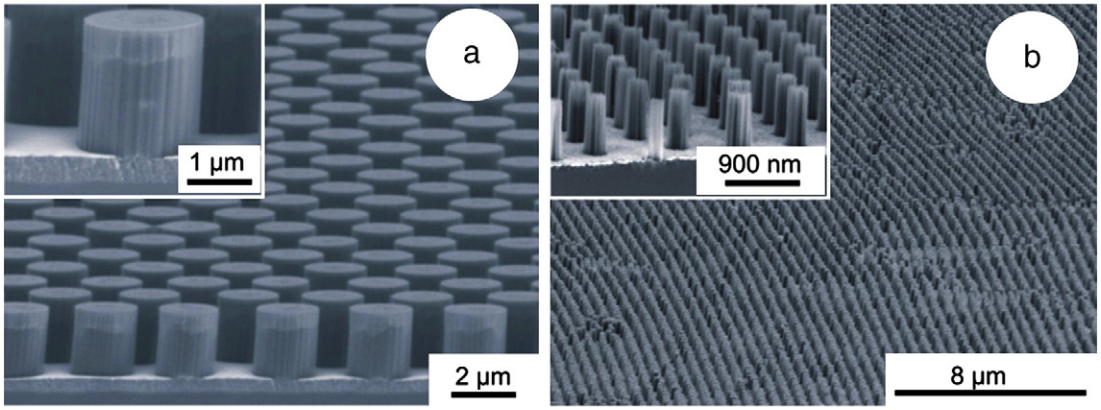

Fig. 8. Cross-section SEM images of Si nanowires fabricated by metal-assisted wet chemical etching. Extended arrays of well-ordered, vertically aligned Si nanowires with controllable diameters can be generated. Si nanowires with diameters of 1.8 µm (a) and 480 nm (b).

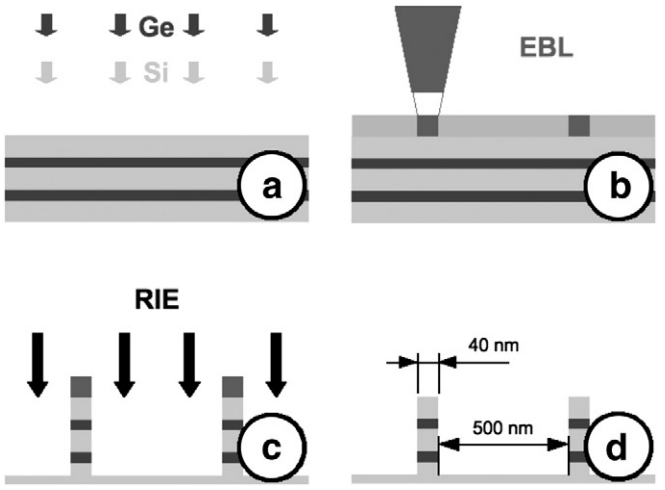

Fig. 9. Schematic diagram of the fabrication process of Si/Ge heterostructure nanowires by molecular beam epitaxy, electron beam lithography and reactive ion etching. At first, the Si/Ge superlattice is grown by molecular beam epitaxy (a). Then, a photoresist is placed on the sample and exposed to an electron beam at defined positions (b). Afterwards, the prepared sample is exposed to a reactive plasma (c). At the end, the remaining photoresist is removed (d).

with mask fabrication by EBL and a RIE step to produce an ordered array of vertical Si/Ge heterostructure NWs.

3.2.1. Experimental details

Like the VLS NWs described above, the Si/Ge superlattice was grown in a Riber SIVA 45 MBE machine (Fig. 9a). Again, a 200 nm Si buffer was deposited first. Then, 30 periods of an alternating sequence of 4 ML Ge and 10 ML Si were grown at 550 °C on the P doped 5″ Si (100) wafer. The growth rates for Si and Ge were 0.05 nm/s and 0.01 nm/s, respectively. At the end, a 20 nm Si capping layer was put on top to protect the superlattice. To prevent the formation of Ge islands, the sample was doped with Sb during growth, which acts as a surfactant. Due to the segregation of Sb, the doping concentration varied from approx. $10^{16}\,cm^{-3}$ at the bottom of the superlattice to approx. $10^{18}\,cm^{-3}$ at the top as measured with secondary ion mass spectrometry on a reference sample.

After the MBE deposition a photoresist was put on top of the superlattice which was then exposed to an electron beam at defined positions in a regular quadratic pattern of spots with a diameter of 40 nm and a distance of 500 nm in between to minimize the proximity effect (Fig. 9b). The overall size of the exposed field was 100 µm × 100 µm. However, this size can be expanded by additional fields. Low-temperature dry etching was applied next to fabricate regular arrays of Si/Ge heterostructure NWs (Fig. 9c). RIE processes in a SF_6/O_2 plasma (R. F. power 40 W, $p = 5\times10^{-6}$ bar) at a substrate temperature of −110 °C were used resulting in etch rates in the order of 60 nm/min. The homogeneous etching of the Si and Ge multilayers was controlled by the SF_6/O_2 ratio and pressure. At the end, the photoresist was removed chemically (Fig. 9d).

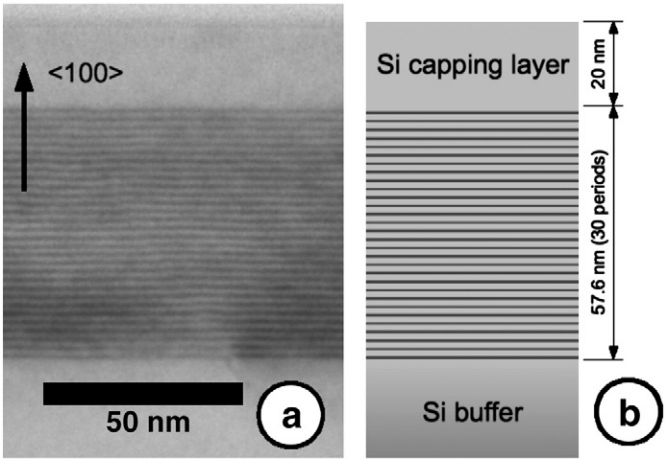

Fig. 10. Comparison of a TEM micrograph of a 30 period Si/Ge superlattice with the calculated model. The individual Ge and Si layers can be clearly distinguished and show a good agreement with the model.

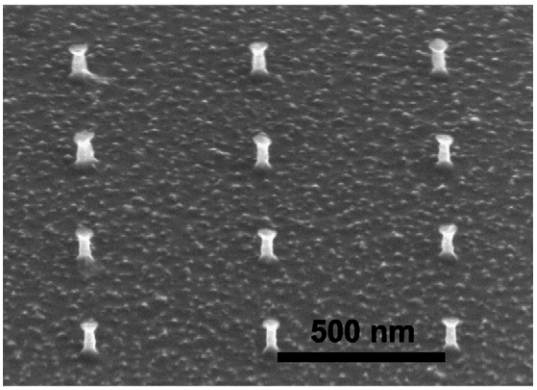

Fig. 11. SEM micrograph of a section of a nanowire array. The original size of the array is 100 µm × 100 µm. The nanowires have a distance of 500 nm. Their diameter varies between 27 nm and 43 nm. Their length is approx. 90 nm. Due to a tilt angle of 52° the nanowires appear shorter than they actually are.

3.2.2. Results and discussions of the reactive ion etching-based approach

In Fig. 10a TEM cross-section micrograph of the superlattice is compared with a model based on the nominal growth rates and the deposition time. The comparison shows the excellent growth control for Si and Ge layers which is possible by MBE and up to now not achieved by any other deposition method. The Si (bright) and Ge (dark) layers can be clearly distinguished. It is difficult to measure the actual Ge concentration within each layer, but the maximum value can be estimated to be larger than 60 at.% to 70 at.% when compared with reference samples.

A part of the NW array etched into the superlattice can be seen in Fig. 11. The SEM micrograph (tilt angle 52°) clearly shows the quadratic arrangement of the NWs and also the constant distance. The NW diameter varies between 27 nm and 43 nm. It can already be seen that there is a certain underetching because the shape of the NWs reminds of mushrooms. However, we are trying to etch NWs with cylindrical shape and straight lateral surfaces, with promising first results for NWs with larger diameters. The last image, Fig. 12, shows a TEM cross-section micrograph of a single nanowire. Again, the Si and Ge layers can be clearly distinguished.

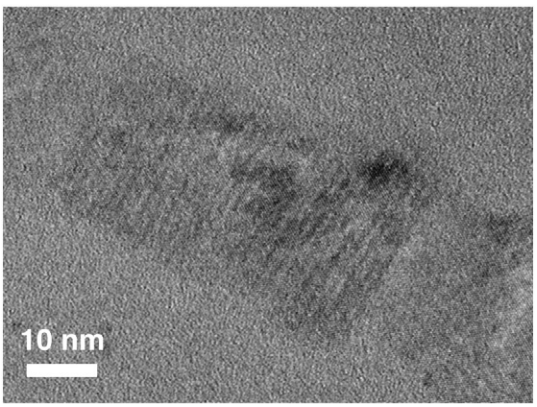

Fig. 12. Cross-section TEM micrograph of a 35 nm diameter nanowire with a Si/Ge superlattice inside. The Ge (dark lines) and Si parts can be clearly distinguished.

3.2.3. Summary and conclusions on the reactive ion etching-based approach

By combining MBE, EBL and RIE, we have fabricated well-ordered arrays of vertical nanowire-based Si/Ge heterostructures which contain a 30 period Si/Ge superlattice with high Ge concentrations and comparatively sharp interfaces. The size of the NW field was 100 μm × 100 μm, but it can be easily expanded. The current set-up of our EBL machine limits the size of the exposed spot of the photoresist to a minimum diameter of 40 nm. Varying the conditions of the dry etch process, a controlled lateral etching results also in a reduction of the NW diameter under the limitation caused by the lithography, although at the cost of a rough and concave surface. We want to emphasize that this method does not involve any metal as catalysts. Therefore the inclusion of any metal atoms as point defects within the NWs can be precluded from the beginning.

As our next steps we want to produce NWs with smaller diameters but smooth surfaces. Furthermore, we plan to study possibilities of passivating the NW surface, embed the NWs in SiO_2 and contact them individually.

4. Comparison of the fabrication approaches

In principle there are two different approaches to fabricate Si NWs and vertical nanowire-based Si/Ge heterostructures: the bottom-up approach and the top-down approach. We presented one bottom-up method and two different top-down methods. The Au catalysed, diffusion-based NW growth by MBE was used to synthesise Si NWs with embedded Ge layers and also Ge NWs on top of Si NWs. These experiments revealed once again that the growth temperature is one of the most crucial parameters. As the first top-down method we presented the fabrication of Si NWs by colloidal lithography and metal-assisted wet chemical etching. In the second top-down method vertical Si/Ge superlattice heterostructure nanowires were produced by a combination of MBE, EBL and reactive ion etching.

Both approaches are interesting from a scientific point of view, for instance to study crystal growth and diffusion mechanisms, and also to investigate the structural, electrical and optical properties of low-dimensional structures compared to the respective bulk values. However, concerning their application potential for future devices, the top-down approach has several advantages over the bottom-up approach. First of all, for top-down approaches it is easier to obtain well-ordered structures, with a high homogeneity in NW diameters and lengths. Especially the MBE/EBL/RIE method also allows the contacting of individual NWs, because the position of each NW is well known. One of the advantages of bottom-up methods was their high NW density, NW length and homogeneous (but statistical) distribution over large areas up to 5″–6″ wafers. Today, this can, for instance, also be achieved by colloidal lithography and wet chemical etching techniques. Furthermore, top-down approaches are independent of the substrate orientation. Depending on their diameter and the underlying substrate, Si NWs grow only in <111>, <110>, and <112> directions. In contrast, vertical <100> NWs on (100) Silicon substrates can be easily produced by etching techniques. (100) Silicon substrates are the most common substrates for industrial applications. Several groups were able to combine both approaches to force Si NWs to grow in an ordered arrangement and/or in <100> direction, e.g. a colloidal mask was used to deposit the Au in a hexagonal arrangement [40], or the NWs were grown within an anodic aluminium oxide membrane on a <100> oriented Si wafer [41,42]. However, as long as the VLS and also the VSS growth depend on a metal droplet or particle as a catalyst, one of the major drawbacks of the bottom-up approach remains. With the possible inclusion of metal catalyst atoms inside the NWs as point defects, which might act as active recombination centres, their application potential, especially for optical devices, is unclear.

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References

[1] N. Usami, T. Mine, S. Fukatsu, Y. Shiraki, Appl. Phys. Lett. 64 (1994) 1126.
[2] Y. Nakajiama, Y. Takahashi, S. Horiguchi, K. Iwadate, H. Namatsu, K. Kurihara, M. Tabe, Appl. Phys. Lett. 65 (1994) 2833.
[3] J.L. Liu, Y. Shi, F. Wang, Y. Lu, R. Zhang, P. Han, S.L. Gu, Y.D. Zheng, Appl. Phys. Lett. 68 (1996) 352.
[4] C.M. Lieber, Mater. Res. Bull. 28 (2003) 128.
[5] H.J. Fan, P. Werner, M. Zacharias, Small 2 (2006) 700.
[6] L.J. Lauhon, Mark S. Gudiksen, C.M. Lieber, Philos. Trans. R. Soc. Lond., A 362 (2004) 1247.
[7] M.S. Dresselhaus, Y.M. Lin, S.B. Cronin, O. Rabin, M.R. Black, G. Dresselhaus, T. Koga, Semicond. Semimet. 71 (2001) 1.
[8] D. Li, Y. Wu, R. Fan, P. Yang, A. Majumdar, Appl. Phys. Lett. 83 (2003) 15.
[9] A.I. Hochbaum, R. Chen, R.D. Delgado, W. Liang, E.C. Garnett, M. Najarian, A. Majumdar, P. Yang, Nature 451 (2008) 163.
[10] L.D. Hicks, M.S. Dresselhaus, Phys. Rev. B 47 (1993) 16631.
[11] A. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W.A. Goddard, J. Heath, Nature 452 (2008) 168.
[12] V. Schmidt, U. Gösele, Science 316 (2007) 698.
[13] S. Kodambaka, J. Tersoff, M.C. Reuter, F.M. Ross, Science 316 (2007) 729.
[14] R.S. Wagner, W.C. Ellis, K. Jackson, S.M. Arnold, J. Appl. Phys. 35 (1964) 2993.
[15] R.S. Wagner, W.C. Ellis, Trans. Metall. Soc. AIME 233 (1965) 1053.
[16] E.I. Givargizov, J. Cryst. Growth 31 (1975) 20.
[17] R.S. Wagner, W.C. Ellis, Appl. Phys. Lett. 4 (1964) 89.
[18] Y. Cui, L.J. Lauhon, M. Gudiksen, J. Wang, C.M. Lieber, Appl. Phys. Lett. 78 (2001) 2214.
[19] J. Westwater, D.P. Gosain, S. Tomiya, S. Usui, J. Vac. Sci. Technol., B 15 (1997) 554.
[20] Y. Wu, Y. Cui, L. Huynh, C.J. Barrelet, D.C. Bell, C.M. Lieber, Nano Lett. 4 (2004) 433.
[21] J. Westwater, D.P. Gosain, S. Usui, Phys. Status Solidi, A 165 (1998) 37.
[22] L. Schubert, P. Werner, N.D. Zakharov, G. Gerth, F. Kolb, L. Long, U. Gösele, T.Y. Tan, Appl. Phys. Lett. 84 (2004) 4968.
[23] H.D. Park, T.P. Hogan, J. Vac. Soc. Technol. B 22 (2004) 237.
[24] P. Werner, N.D. Zakharov, G. Gerth, L. Schubert, U. Gösele, Int. J. Mat. Res. 97 (2006) 7 formerly Z. Metallkd.
[25] N.D. Zakharov, P. Werner, G. Gerth, L. Schubert, L. Sokolov, U. Gösele, J. Cryst. Growth 290 (2006) 6.
[26] R. Dujardin, V. Poydenot, T. Devillers, V. Favre-Nicolin, P. Gentile, A. Barski, Appl. Phys. Lett. 89 (2006) 153129.
[27] L. Schubert, Doctoral Thesis, Martin Luther University Halle-Wittenberg, 2006 (in German).
[28] B. Predel, H. Bankstahl, T. Gödecke, J. Less-Common Met. 44 (1976) 39.
[29] C.B. Collins, R.O. Carlson, C. Gallagher, J. Phys. Rev. 105 (1957) 1168.
[30] J.E. Allen, E.R. Hemesath, D.E. Perea, J.L. Lensch-Falk, Z.Y. Li, F. Yin, M.H. Gass, P. Wang, A.L. Bleloch, R.E. Palmer, L.J. Lauhon, Nat. Nanotech. 3 (2008) 168.
[31] S.H. Oh, K. van Benthem, S.I. Molina, A.Y. Borisevich, W. Luo, P. Werner, N.D. Zakharov, D. Kumar, S.T. Pantelides, S.J. Pennycook, Nano Lett. 8 (2008) 1016.
[32] M.C. Putnam, M.A. Filler, B.M. Kayes, M.D. Kelzenberg, Y. Guan, N.S. Lewis, J.M. Eiler, H.A. Atwater, Nano Lett. 8 (2008) 3109.
[33] J.C. Hulteen, D.A. Treichel, M.T. Smith, M.L. Duval, T.R. Jensen, R.P. Van Duyne, J. Phys. Chem., B 103 (1999) 3854.
[34] C.L. Cheung, R.J. Nikolić, C.E. Reinhardt, T.F. Wang, Nanotechnology 17 (2006) 1339.
[35] K. Peng, M. Zhang, A. Lu, N. Wong, R. Zhang, S. Lee, Appl. Phys. Lett. 90 (2007) 163123.
[36] Z.P. Huang, H. Fang, J. Zhu, Adv. Mater. 19 (2007) 744.
[37] X. Li, P.W. Bohn, Appl. Phys. Lett. 77 (2000) 2572.
[38] R. Douani, K. Si-Larbi, T. Hadjersi, N. Megouda, A. Manseri, Phys. Status Solidi, A 205 (2007) 225.
[39] C. Chartier, S. Bastide, C. Lévy-Clément, Electrochim. Acta 53 (2008) 5509.
[40] B. Fuhrmann, H.S. Leipner, H.-R. Höche, L. Schubert, P. Werner, U. Gösele, Nano Lett. 5 (2005) 2524.
[41] T. Shimizu, T. Xie, J. Nishikawa, S. Shingubara, S. Senz, U. Gösele, Adv. Mater. 19 (2007) 917.
[42] T. Shimizu, Z. Zhang, S. Shingubara, S. Senz, U. Gösele, Nano Lett. 9 (2009) 1523.