A pure 1.5 μm electroluminescence from metal-oxide-silicon tunneling diode using dislocation network

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This letter has demonstrated a light emitting diode (LED) with a pure 1.5 μm emission using a metal-oxide-silicon (MOS) tunneling structure based on dislocation network in direct silicon bond wafer. It is found that under negative gate bias, the electrons in the metal gate electrode tunnel through the thin oxide to silicon and then recombine radiatively with holes at the dislocation related states to emit the D1-line with a wavelength of 1.5 μm. The calculation of energy band diagram indicates that a potential well for electrons forms at the charged bonding interface under negative bias, therefore, the electrons tunneled from the gate can rapidly be attracted by the electric field and then confined at the interface, which essentially increases the efficiency of D1 luminescence from MOS tunneling LED. These results are of interest for the development of silicon based photonics with 1.5 μm light emission. © 2008 American Institute of Physics. [DOI: 10.1063/1.2965126]

The conventional metal lines in the ultralarge scale integration have faced serious problems, such as heat penalty, nonacceptable delay, and cross talk. The optical interconnects are expected to replace them and drive the continued developments in silicon. Light emission from silicon is the most interesting topic because the extensive experience in silicon fabrication and processing could be put to best use. However, a complementary metal-oxide-semiconductor compatible electrically pumped Si-based light emitting diode (LED) is still lacking, even though different approaches for light emitters have intensively been studied. The desired light emitter should not only exhibit a high luminescence efficiency, but also be spatially confined and emit at about 1.5 or 1.3 μm. LEDs based on erbium-doped layers consisting of silicon nanoparticles embedded in silicon oxide or silicon nitride, respectively, are known to emit at 1.55 μm, which need a rather high bias voltage to cause efficient electroluminescence (EL). Another LED exhibiting 1.5 μm light emission with efficiency of 1% at room temperature has been fabricated based on the dark emission from silicon and then recombine radiatively with holes at the dislocation related states to emit the D1-line with a wavelength of 1.5 μm. The calculation of energy band diagram indicates that a potential well for electrons forms at the charged bonding interface under negative bias, therefore, the electrons tunneled from the gate can rapidly be attracted by the electric field and then confined at the interface, which essentially increases the efficiency of D1 luminescence from MOS tunneling LED. These results are of interest for the development of silicon based photonics with 1.5 μm light emission. © 2008 American Institute of Physics. [DOI: 10.1063/1.2965126]
high probability of carriers tunneling. Figure 1(b) shows the plane-view TEM micrograph of dislocation network at the bonding interface. It can be seen that the network consists of screw and edge dislocations. Generally, the structure of a dislocation network, i.e., the density and type of formed dislocations, depends on the disorientation angles during wafer bonding.\(^\text{12}\) The spacing (\(d\)) of adjacent screw/edge dislocations calculated according to \(d = b \cdot \sin(\alpha \text{ or } \beta)\) (\(b\) is Burgers’ vector of dislocation),\(^\text{13}\) are respectively in agreement with the value of 17 and 20 nm shown in TEM micrograph. Therefore, it is believed that the structure of dislocation network can be well reproduced by controlling the disorientation angles during bonding.

Figure 2 shows the \(I-V\) curve of dislocation related MOS diode as well as the referenced one. Note that both MOS diodes exhibit the similar \(I-V\) characteristics. A significant current was seen under negative gate bias due to holes tunneling from the \(p\)-type silicon to Ti gate and the electrons tunneling from the Ti gate to the substrate. The very weak voltage dependence of the reverse current under positive gate bias was seen under negative gate bias due to holes tunneling from the Ti gate to the substrate. The very weak reverse current is obviously controlled by the thermal generated holes.\(^\text{14}\)

When a significant current flows through the diodes under negative gate bias, the pure 1.5 and 1.1 \(\mu m\) light was observed from the dislocation related MOS diode and the referenced one, respectively. Figure 3(a) shows the EL spectra of dislocation related MOS diode under different negative gate bias at 77 K and the inset is an EL spectrum of referenced MOS diode. The 1.5 \(\mu m\) light is obviously emitted from the dislocation network at the bonding interface, which is so called D1-line.\(^\text{15}\) Since the dislocation related MOS diode only emits the dislocation related luminescence without the existence of band-to-band luminescence, it can be deduced that when a dislocation network is located in the near-surface region of MOS diode, the carrier recombination at the dislocation related states at the bonding interface can completely take over the carrier transition between conduction and valence bands for the 1.1 \(\mu m\) emission (B-B line). The reason will be explained by energy band diagram later. The increase of D1-line intensity with negative bias in Fig. 3(a) is consistent with the increase of tunneling current. Figure 3(b) shows the luminescence spectra from the dislocation network at different temperatures. The observed redshift of D1-line with the increase of temperature is due to the temperature dependence of silicon band gap \(E_g\) which obeys the law of \(E_g(T) = 0.34\ \text{eV}\), see the inset in Fig. 3(b). This suggests that if the carrier transition for D1-line takes place on single level related to dislocations, it should be around \(E_g + 0.34\ \text{eV}\), which was often reported by DLTS measurement for plastically deformed silicon.\(^\text{16}\) Even though the D1-line was not observed at room temperature, it should be achievable using MOS diode since the most of the light has been blocked by the thick Ti gate electrode and only the emission from the diode edge could be detected. Nevertheless, we still estimated the emission efficiency of our dislocation related MOS-LED at 77 K by comparing the present EL intensity under forward bias with that of a silicon \(p-n\) diode and obtained an efficiency value of about 0.1\% for the 1.5 \(\mu m\) emission. As the D1-line originates from the radiative recombination of carriers at the dislocation related interfacial states, the distribution of electrons and holes at the bonding interface in the MOS diode under negative gate bias is essentially important.

The capacitance (\(C\)) of the dislocation related MOS diode obtained at high frequency is contributed by the thin oxide and the space charge region (SCR) in silicon, which can be expressed by\(^\text{17}\)

\[
C = \frac{1}{\varepsilon_{\text{Si}} A} \left( \frac{d_1 + d_2}{\varepsilon_{\text{Si}} A} + \frac{d_{\text{ox}}}{\varepsilon_{\text{ox}} A} \right) \tag{1}
\]

where \(\varepsilon_{\text{Si}}\) and \(\varepsilon_{\text{ox}}\) are the dielectric constant of silicon and silicon oxide, respectively, \(A\) is the Ti gate area, \(d_1\) and \(d_2\) are
the widths of SCR on each side of bonding interface, respectively, and $d_{ox}$ is the oxide thickness. If neglecting the charges at the silicon/oxide interface, the charge density at the bonding interface $N_{ss}$ is to be balanced by that within the silicon’s SCR $N_{sc}$ and that on the Ti gate $N_{m}$, as follows:

$$qN_{ss} = -(qN_{sc} + qN_{m}) = qN_{s}(d_1 + d_2) - qN_{n},$$

where $q$ is unit charge and $N_{s}$ is the dopant concentration. Then, according to Poisson’s equation and Gauss’ law, the potential dropping on different regions of the MOS diode under external gate bias $U$ can be written as

$$V_{ox} = -\frac{q^2N_{m}d_{ox}}{e_{ox}}; \quad V_1 = -\left(\frac{q^2N_{m}d_1}{e_{ox}} - \frac{q^2N_{s}d_1}{2e}\right),$$

$$V_2 = -\frac{q^2N_{s}d_2}{2e},$$

$$qU + V_0 + V_{ox} + V_1 + V_2 = 0,$$

where $V_0$ is the built-in potential barrier between the Ti gate and the present silicon, $V_{ox}$ is the potential distribution on the oxide, and $V_1$ and $V_2$ are the SCR on the left and right side of bonding interface, respectively. After measuring the capacitance $C$, the charge density at the Ti gate and bonding interface, and the potential distribution in the MOS diode under different gate bias can be obtained, based on Eqs. (1)–(4).

The results indicate that with the increase of negative gate bias, the potential distribution on the oxide becomes larger and therefore results in an increase of probability of electron tunneling through the oxide. Figures 4(a) and 4(b) show the energy band diagrams of our dislocation related MOS diode under gate bias of 0 and −2 V, respectively. Note that Fermi level on the right side of bonding interface connecting with positive electrode, shifts downward with the increase of negative gate bias. Some interface states with energies below Fermi level under zero bias go above the Fermi level and capture holes to increase the charge density at the bonding interface. Since the Fermi level is pinned by the interface states with a large state density of $10^{12}$–$10^{13}$ cm$^{-2}$ eV$^{-1}$, which is estimated from the dependence of interfacial charge density on Fermi level, the negative bias only causes a severe band bending on the left side of bonding interface, while the band bending on the right side is less dependent on negative bias. As a consequence, the hole current, depending on the barrier height on the right side of the bonding interface, does not change much, and the increase of measured current with negative gate bias in Fig. 2 is mainly attributed to electrons tunneling from the Ti gate to silicon. Thus, we can conclude that the increase of our D1-line with negative bias observed in Fig. 3(a) is a result of the electron (minority carrier) current increasing. Meanwhile, note that a significant potential well for electrons forms at the bonding interface by the band bending on the left side of the bonding interface under negative bias and the electric field induced by the charged interface increases with negative gate bias. Therefore, once electrons tunnel through the thin oxide, they will be attracted rapidly to the positively charged bonding interface by the strong electric field and then confined in the potential well. This essentially makes the tunnelled electrons give the largest contribution to D1-line generation at the interface states related to dislocations and the direct recombination between holes and electrons for B-B luminescence is difficult to take place.

In conclusion, we have reported a pure 1.5 μm light emission from a MOS tunneling diode using dislocation network in a p-type DSB wafer. Under negative bias, electrons can tunnel through the thin oxide from the metal gate to p-type silicon and attracted rapidly by the charged bonding interface. Then the electrons radiatively recombine with the holes at the dislocation related states to emit the D1 luminescence at 1.5 μm. A calculation of energy band diagram near the bonding interface shows that a potential well forms at the interface states which induces the largest probability of D1 luminescence generation without the band-to-band luminescence.

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