Characteristics of Al₂O₃/AlInN/GaN MOSHEMT

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InAlN/GaN is a new heterostructure system for HEMTs with thin barrier layers and high channel current densities well above 1 A/mm. To improve the leakage characteristics of such thin-barrier devices, AllnN/GaN MOSHEMT devices with a 11 nm InAlN barrier and an additional 5 nm Al₂O₃ barrier (deposited by ALD) were fabricated and evaluated. Gate leakage in reverse direction could be reduced by one order of magnitude and the forward gate voltage swing increased to 4 V without gate breakdown. Compared to HEMT devices of similar geometry, no degradation of the current gain cutoff frequency was observed. The results showed that InAlN/GaN FETs with high channel current densities can be realised with low gate leakage characteristics and high structural aspect ratio by insertion of a thin Al₂O₃ gate dielectric layer.

Introduction: Recently, it has been shown that AllnN/GaN HEMTs can operate at high current densities well above 1 A/mm, with high speed and at high temperature [1–4]. With 17% In-content in the barrier the heterostructure is lattice matched and highly stable, while barriers as thin as about 10 nm can be used. These thin barriers might give rise to higher gate leakage current levels as compared to AlInN/GaN HEMT devices. This might be a limitation to the high-voltage/high-power operation, although the critical breakdown field of InAlN should be higher than that of AlInN. To improve the gate leakage in such HEMT devices, thin oxide barriers could be inserted, resulting in a MOSHEMT structure. The insertion of such a layer, however, might substantially degrade the structural aspect ratio, which is necessary to preserve the gate control capability. The thin InAlN barriers allow for the insertion of thin Al₂O₃ oxide layers, while still maintaining a high aspect ratio. Such a structure will be discussed below. Al₂O₃ material offers the advantages of a large bandgap (>9 eV), high dielectric constant (k~10), high breakdown field (~10⁶ V/cm), thermal stability (amorphous up to 1000°C) and chemical stability [5].

Material growth and device fabrication: An AIXTRON metal organic chemical vapour deposition system was used to grow AlInN/GaN on two-inch diameter (0001) sapphire substrates. The studied structures consisted of a 3 µm-thick GaN buffer, a 1 nm-thick AlInN spacer layer and an 11 nm-thick AllnN barrier layer with 82% Al content measured by X-ray diffraction. Hall effect measurements at room temperature showed a sheet carrier density Nₛ = 1.9 × 10²⁸ cm⁻², a sheet resistance of 330 Ω/sq. and a mobility of 1230 cm²/Vs. FETs were realised as follows: MESA isolation was performed by dry etching. For the ohmic contacts, we used a Ti/Al/Ni/Au metal stack annealed at 870°C for 30 s. We obtained contact resistances Rₛ = 0.6 Ω mm by TLM measurements. The drain-source distance was 3 µm. The wafer was divided into two parts. The gate was deposited directly onto the AllnN barrier layer (Fig. 1a) of the first half wafer. A 5 nm amorphous Al₂O₃ oxide layer was deposited onto the second half by atomic layer deposition (ALD) prior to the gate processing (Fig. 1b). The ALD technique allows high-quality ultra-thin material deposition with atomic layer accuracy. Ni/Au Schottky gates were defined by e-beam lithography with different lengths of 0.2, 0.35 and 0.7 µm. The gate width was 100 µm. They were placed asymmetrically between drain and source, 1 µm apart from the source contact. The devices were unpassivated.

Device performance: Fig. 2 shows the gate leakage current as a function of the gate-source bias of the AlInN/GaN HEMTs and MOSHEMTs with identical geometry (0.2 × 100 µm²). As expected, the Al₂O₃ MOSHEMTs exhibit a lower gate leakage current density (about one order of magnitude) than the conventional HEMTs. This leads to an increase of the two-terminal reverse breakdown voltage (about 25%) and of the forward breakdown voltage (about 30%). This confirmed that the Al₂O₃ dielectric thin film acts as an efficient gate insulator. Fig. 3 shows typical output characteristics of AllnN/GaN HEMTs and MOSHEMTs, respectively. The HEMTs and MOSHEMTs were completely pinched-off at a gate voltage of ~4 and ~8 V, respectively. The negative shift in the threshold voltage was attributed to the decreased gate barrier capacitance. The experimental threshold voltage for both HEMTs and MOSHEMTs were in good agreement with the values obtained from (1), neglecting the residual doping in the InAlN barrier layer [6]:

\[ V_{th} = \frac{e n_s}{C_b} \]  

where \( e \) is the electronic charge, \( n_s \) is the sheet charge density and \( C_b \) is the total unit area capacitance of the barrier layer and dielectric. The transconductance was reduced from 220 to 185 mS/mm. This was in agreement with an estimated reduction of 20%, assuming drift velocity saturation (at \( L_d = 0.2 \mu m \)) with \( v_{dsat} \approx 5 \times 10^7 \) cm/s.

The maximum drain current density was \( I_{Dmax} = 1.15 A/mm \) for HEMTs at \( V_{GS} = +2 V \). The moderate maximum current density was mainly caused by the moderate sheet charge density. Above \( V_{GS} = +2 V \) the gate diode leakage current became pronounced as seen near the origin of the output characteristics. Thus, the maximum output current was limited by the gate diode characteristics and not by the unpassivated channel part between source and gate, which could act as a current limiter also degrading the transfer characteristics. In the case of the MOSHEMTs, a low gate leakage current was observed up to \( V_{GS} = +4 V \). At this gate...
bias the channel current was slightly increased to 1.3 A/mm, but the
transfer characteristics showed increasingly $g_m$-compression. This indi-
cates that the maximum channel current was now more limited by the
channel cross-section between gate and source and less by gate leakage.
This also allows us to estimate the potential of the oxide covered surface
between gate and source to be very low (less than 0.3 eV). Further
investigations will be performed in order to extract the gate diode barrier
height and the surface potential of both HEMTs and MOSHEMTs more
precisely.

Fig. 4 shows the current gain cutoff frequency as a function of $1/L_G$, where $L_G$ is the gate length. An $F_T$ of 53 GHz could be extracted for a
gate length of 0.2 μm. The $F_T \times L_G$ product calculated from the data
points was approximately 10.5 GHz μm and independent of the device
configuration. This indicates that the high aspect ratio of both structures
may allow the realisation of FETs with even shorter gate length without
high-frequency degradation. The MOSHEMT structure presents the
additional advantage of the suppression of gate leakage, which
normally increases as the gate length becomes shorter.

![Image](image_url)

**Fig. 4** Current gain cutoff frequency according to gate length of AlInN-
GaN HEMT and MOSHEMT biased at drain–source voltage of 10 V
Inset: typical cutoff frequency of 0.2 × 100 μm AlInN/GaN MOSHEMT

Conclusions: Al$_2$O$_3$/AlInN/GaN MOSHEMTs present a significant
reduction of the gate leakage current, an increase of the maximum
drain current density by operating at high forward gate bias and no
degradation of small-signal parameters compared to conventional
AlInN/GaN HEMTs. A reduced transconductance of the MOSHEMT
was observed owing to the use of identical heterostructure design. To
further improve the DC and RF characteristics of the MOSHEMT, the
thickness of the AlN barrier may be further decreased below 10 nm
and the gate length reduced to maintain the structural aspect ratio.

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