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Synthesis of Vertical High-Density Epitaxial Si(100) Nanowire Arrays on a Si(100) Substrate Using an Anodic Aluminum Oxide Template**

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Because of their unique electrical and optical properties, Si nanowires have attracted considerable attention, and already a number of devices based on Si nanowires as building blocks have been demonstrated.[1–4] Nanowires grown by using the vapor–liquid–solid (VLS) technique have been shown to have advantages compared with conventional lithographic techniques in terms of well-defined surface, small minimum size, and fabrication cost. Additionally, the VLS technique can be used to prepare epitaxially grown nanowires on single-crystal substrates. Vertically standing epitaxial nanowires as a device platform[3,4] avoid pick-and-place approaches or nanomanipulations. For vertical devices, control of growth direction and crystallographic orientation of the nanowire are important parameters.

In order to combine vertically grown epitaxial Si nanowires with conventional Si micro/nanoelectronics manufactured on Si(100) wafers, the most important issue is the realization of vertically grown epitaxial Si nanowires, along the [100] direction, on Si(100) substrates. Epitaxial Si nanowires grown without any template on Si substrates reported up to now have three preferred growth directions, in particular <111>, <112>, and <110> depending on the diameter of the wires.[5] Based on the present knowledge the preferred growth directions are <111> for large diameter nanowires and <112> and <110> for small diameters, independent of the growth method, if no template is used. In this paper, we utilize an anodic aluminum oxide (AAO) template with vertical nanopores to grow epitaxial Si(100) nanowires on a Si(100) substrate.

AAO is known to have ordered honeycomb nanopore arrays, perpendicular to the substrate. The diameter and the density of the nanopores can be controlled from a few nanometers to several hundred nanometers and several 10^9–10^{12} pores inch^{-2} (1 inch ≈ 2.54 cm) depending on the anodic voltage and acid species used for anodic oxidation.[6–9] AAO has, therefore, been used as a template to prepare nonepitaxial nanowires[10] and nanotubes of various materials[11,12] or as a mask to form nanodot arrays.[13,14] Generally, it is difficult to obtain epitaxial growth of embedded material in the AAO nanopores, as an amorphous layer called the "barrier layer", exists at each nanopore bottom. There are, mainly, two approaches to remove the AAO barrier layer. One method is to separate the AAO membrane from the Al bulk by selective chemical etching of Al. After that, the end of the AAO membrane with the barrier layer is etched away, and continuous pores are prepared.[13,14] Putting this AAO membrane on a substrate, it can be used as shadow mask for evaporation to form nanodot arrays directly on the substrate. Lombardi et al.[13] prepared Au nanodot arrays on a Si(111) substrate by using this method. They utilized the Au dots as a catalyst for VLS growth of Si after removal of the AAO membrane from the substrate. They succeeded in preparing a vertically grown epitaxial Si(111) nanowire array of 39×10^9 wires inch^{-2} with uniform diameter and spacing on a Si(111) substrate. Another approach utilizes a thin aluminum film on a conductive substrate. The electrochemical formation of aluminum oxide stops as soon as all Al metal is consumed. The thinner AAO barrier formed on the conductive material is removed by chemical etching.[15–17] In this case, the AAO membranes are fixed to the substrate. This is a big advantage compared with the first approach because it is possible to use the AAO nanopores as a template to control the growth direction of nanowires perpendicular to the substrate surface, even if the direction is not a preferred orientation of nanowire growth. Our previous study demonstrated epitaxially grown Si(100) nanowires on Si(100) substrates using AAO templates fixed on the substrate, which had a catalyst Au film sandwiched between the AAO membrane and Si substrate.[18] However, only up to 30 % of the nanopores were filled with nanowires, because the Au–Si eutectic did not fill every nanopore.

In this paper we describe a new approach. First, as presented before, AAO nanopores on a Si substrate are produced. After etching away the AAO barrier layer at the bottom of the pores Au is deposited inside the pores with direct contact to the Si substrate. One well-established method to deposit metal nanowires into the AAO nanopores is pulsed electrodeposition.[19] This allows metal nanowires with almost

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identical length in all nanopores to be obtained, because during each pulse a small amount of metal is deposited. This works even if a thin oxide layer remains between substrate surface and metal nanowire. In our experiment a direct contact between catalyst Au and Si surface is essential to obtain epitaxial growth of Si nanowires. The Si surface at the AAO nanopore bottom is known to be covered by a thin oxide layer.[20,21] Removal of this bottom oxide layer is possible, by pre-annealing the AAO template in inert gas and later immersion in HF acid.[17] Furthermore, we can use electroless deposition of Au, with a gold solution containing HF. Synthesis of epitaxial Si(111) nanowires using electroless deposition of Au without HF acid has already been demonstrated by Yasseri et al.[22] These authors proved the importance of a direct contact between deposited Au and Si substrate to obtain epitaxial growth of Si nanowires. Our electroless deposition solution containing HF acid is expected to realize both a stable oxide-free silicon surface at the nanopore bottom and a selective Au deposition on the Si substrate. In this study, because of the aim of realizing dense epitaxial Si(100) nanowires on a Si(100) substrate, we combined electroless deposition of Au into AAO nanopores and VLS growth of Si.

AAO templates were obtained by anodization of Al films on Si substrates. At first, we prepared Al films deposited by electron-beam evaporation (thickness ca. 2000 nm) on H-terminated n-type Si(100) substrates (resistivity less than 60 mΩ cm) as anode. The electrical contact was made from the back side of the Si substrate during anodic oxidation. The Al films were anodized in an electrolyte based on oxalic acid (0.3 M $H_2C_2O_4$ with deionized water) at 40 V with a two-step anodization technique.[23] The first anodization was stopped when the thickness of the rest of the Al film on the Si substrate reached about 500 nm. After selective etching the first AAO film by using wet chemical etching, a second anodization was performed to transform the rest of the Al into AAO. Then, in order to remove the thinned AAO bottom barrier layer, we slightly etched the aluminum oxide with diluted phosphoric acid. At this point, although the Si surface at each nanopore bottom was still covered by a silicon oxide film, we obtained an AAO template, whose diameter of nanopores was wider at the bottom than at other positions, without an AAO barrier layer on the Si substrate.

We tried to remove this remaining silicon oxide layer by using HF treatment. However, HF treatment etches not only SiO_2, but also the AAO template. It was, therefore, important to investigate and improve the resistance of AAO against HF, because we would be using a HF-containing solution for removal of the oxide layer on the Si surface and electroless deposition of Au into nanopores. AAO templates were pre-annealed in Ar gas for 3 h at different temperatures. Figure 1 shows the pre-annealing temperature dependence of the AAO etching rate with diluted HF. The etching rates were evaluated by comparing the average diameter of nanopores before dipping into diluted HF, with diameters after dipping. The etching rate decreased with increasing pre-annealing temperature, and the AAO was hardly etched after pre-annealing above about 800 °C.

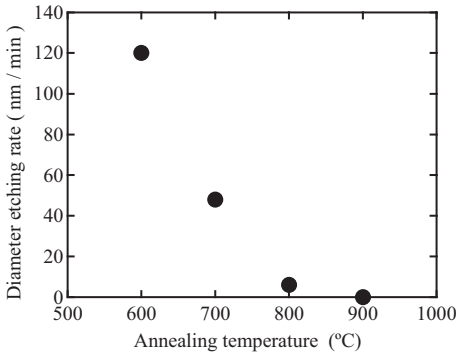

Figure 1. Dependence of HF etch rate of the AAO as a function of its pre-annealing temperature. Etching conditions: 30 °C, 1 % HF solution.

Figure 2 shows a schematic drawing of a cross-section of the synthesis process of Si nanowire arrays in AAO nanopores. The HF treatment was performed for AAO templates pre-annealed at 900 °C. We dipped AAO templates into diluted HF solution (15 min, 1 %, at room temperature). Subsequently, Au particles were embedded in each nanopore by using electroless Au deposition with a mixture of 20 mL 0.02 M $KAuCl_4$ and 18 mL 49 % HF. The mechanism of the electroless metal deposition on Si substrates from HF solution was discussed in the literature as galvanic displacement reactions.[24,25] Exchanging electrons through the Si substrate, the reduction of metal ions as cathodic process and the oxidation of Si atoms as anodic process occur simultaneously at the Si surface.

The HF-containing electroless deposition solution stabilizes the H-termination of the Si surface at the bottom of the AAO nanopores, and then the Au nucleation immediately occurs on the Si surface. These Au nuclei provide electrons to Au ions because they collect more electrons from the Si substrate. Au atoms are preferentially deposited around the nucleation sites, where the nuclei become larger and connected to each other. On the pre-annealed AAO surface consisting of Al_2O_3, an oxidation and displacement process to produce electrons should not occur. As a result, the deposition of Au selectively takes place on the Si surface. We performed electroless de-

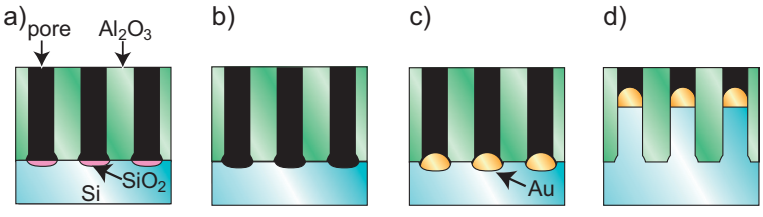

Figure 2. Schematic cross-sectional drawing of the growth of Si nanowires in AAO nanopores using Au nanoparticles as the catalyst: a) after pre-annealing at 900 °C, b) after HF etching to remove SiO_2, c) electroless Au deposition, and d) VLS growth of Si nanowires.

position until the average height of Au reached about half the pore diameter.

Starting with the AAO templates containing Au, Si nanowires were produced by using ultrahigh-vacuum (UHV) chemical-vapor deposition using diluted silane gas as a precursor. The Au particles in the nanopore served as a catalyst, and silane gas accessed Au through the open end of the AAO nanopores. Growth of Si nanowires was carried out at a temperature of 490 °C and a total pressure of 0.80 mbar. The gas was a mixture of 5 % silane and 95 % Ar. We stopped this process before Si nanowires grew out from the nanopores. For the scanning electron microscopy (SEM) observation, the AAO template was selectively etched by phosphoric acid at 100 °C for 60 min. A cross-sectional transmission electron microscopy (TEM) specimen was prepared from the sample with the AAO template.

Figure 3 shows SEM images of Si nanowires after selective etching of AAO template with 60° tilt. We can see a dense array of Si nanowires capped by Au particles on their top, which

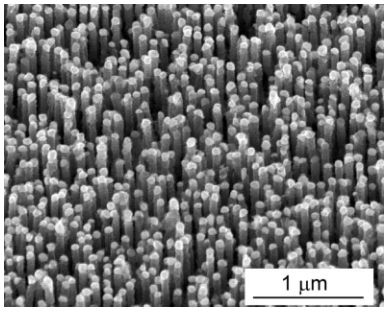

Figure 3. Side-view SEM image with 60° tilt of Si nanowires after selective etching of the AAO template by using phosphoric acid.

grew vertically, parallel to Si [100], perpendicular to the surface of the Si(100) substrate. The average diameter of the nanowires is about 60 nm, fitting the nanopore size of the AAO template. The density of these nanowires, estimated from top-view SEM images, is 69×10^9 wires inch^{-2}, indicating that more than 90 % of the nanopores were filled with Si nanowires.

Figure 4a shows a cross-sectional TEM image of the lower part of a Si nanowire in the AAO nanopores, and the Fourier transformation for the lower part of the Si nanowire including the substrate is shown in the inset. Further, the original position of the surface of the Si substrate is shown as a dashed line in Figure 4a and b. Because of the shape of the AAO nanopore, the diameter of the lower part of the Si nanowire, near the Si substrate, is larger than in the upper part. Upon heating above the eutectic temperature (363 °C), the Au deposited on the Si substrate inside the AAO nanopore makes a liquid eutectic with Si. This eutectic acts as a catalyst during VLS growth and cracks the silane gas. The Si atoms originating from the silane vapor diffuse through the supersaturated liquid eutectic, and freeze out at the liquid–solid interface. By a continuation of this process, the droplet is displaced and

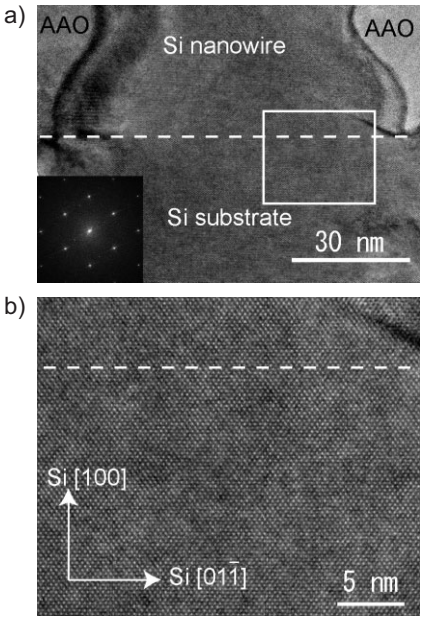

Figure 4. Cross-sectional TEM image of Si nanowire in the AAO template along the [011] zone axis. The dashed line shows the surface position of the original Si substrate. a) Lower part of the Si nanowire and Si substrate. The content of the white box is shown in (b). The inset shows the Fourier transformation of a square region of (a). b) High-resolution TEM image of the interface of substrate and deposited Si demonstrating epitaxial growth.

moves upward from the substrate along the nanopores. The shape of the droplet changes to fit the nanopore diameter. Thus the diameter of the interface of liquid–solid is decreased with increasing height during the first growth stage, whereas a nanowire with a constant diameter grows in the upper region of the nanopore with constant diameter. The nanopore guides the growth direction of the wire along the pore direction. If we continued the nanowire growth beyond the thickness of the AAO template, the nanowires would grow along their preferred growth directions after loosing the guidance from the pore walls.[18]

Figure 4b shows an enlarged image of the interface between the Si substrate and the Si grown by using the VLS process, indicated as a box in Figure 4a. Here, we assume that the real interface between the Si substrate and the nanowire is around 5–15 nm below the original Si surface (shown as dashed line in Fig. 4b) at the nanopore bottom, because of the dissolution of SiO_2 during HF dipping and electroless Au deposition containing HF acid.[20,25] The lattice planes of the Si substrate continuously extend into the wire without any oxide layer. Furthermore, the Fourier transformation spots show only the pattern typical for single-crystal Si along the [011] zone axis. These results suggest that this nanowire is grown homoepitaxially on the Si(100) substrate, and the growth direction is parallel to the substrate [100] direction. Additionally, all nanowires that were observed in this TEM specimen (more than 20 wires) were grown epitaxially.

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The crystalline quality of Si nanowires is better than that achieved by using our previous synthesis method,[18] because the density of defects located at the interface between the original Si substrate and the nanowires was considerably reduced. The HF acid efficiently worked to produce a clean surface of Si at each nanopore bottom and a direct contact between substrate and deposited Au was obtained. Furthermore, several bicrystalline Si nanowires containing {111} twin boundaries were observed. For clarification of whether the mechanism of fabrication of twins is related to the AAO nanopore, changing the growth conditions would be necessary, like growing Si nanowires on other index substrates. The formation of twins was already observed in free-standing Si nanowires (see, for example, Wang et al.[26]).

The synthesis of vertically grown epitaxial Si nanowires has been demonstrated using an AAO template and the VLS technique. Electroless deposition of Au with HF acid efficiently worked to give direct contact between deposited Au and the Si substrate at each nanopore bottom, which helped to grow Si nanowires with high crystalline quality. The method described in this paper allows, using the substrate properly cut in the desired orientation, selecting the crystal orientation of nanowires grown perpendicular to the surface of the substrate. It could be easily extended to realize a range of diameters between 10–20 nm and higher-density nanowire arrays by changing the acid from oxalic to sulfuric acid and using a lower anodization voltage. A further decrease of the diameter of the Si nanowires can be accomplished by controlled thermal oxidation of the free-standing wires and subsequent etching away of the resulting SiO_2 coverage.[27]

Experimental

Al films were deposited by using electron-beam evaporation (thickness ca. 2000 nm) on H-terminated n-type Si(100) substrates (resistivity less than 60 mΩ cm) as anode. Electrical contact of the back side was made by pressing the Si substrate to a Cu block. The temperature of the Cu block was maintained at 3 °C. The Al films were anodized in an electrolyte based on oxalic acid (0.3 M $H_2C_2O_4$ with deionized water) at 40 V with a two-step anodization technique [23]. The first anodization was stopped when the thickness of the rest of the Al film on the Si substrate reached about 500 nm. After selective etching of the first AAO film by wet chemical etching (30 min, 60 °C, mixture of 6 wt % phosphoric acid and 1.8 wt % chromic acid) a second anodization was performed until a sudden decrease of the current was observed. Then, we slightly etched the aluminum oxide with diluted phosphoric acid (20 min, 30 °C, 5 %). At this point, although the Si surface at each nanopore bottom was still covered by a silicon oxide film, we obtained an AAO template, whose diameter of nanopores was wider at the bottom than at other positions, without an AAO barrier layer on the Si substrate.

The AAO templates were pre-annealed in Ar gas (3×10^{-3} mbar, 99.995 %, background pressure 1×10^{-6} mbar; 1 bar = 100 000 Pa) for 3 h at 900 °C. We dipped the AAO templates into diluted HF solution (15 min, 1 %, at room temperature). Subsequently, Au particles were embedded in each nanopore by using electroless Au deposition with a mixture of 20 mL 0.02 M $KAuCl_4$ and 18 mL 49 % HF.

The samples were transferred into the UHV system. Growth of Si nanowires was carried out at a temperature of 490 °C and a total pressure of 0.80 mbar. The gas was a mixture of 5 % silane and 95 % Ar.

Selective etching of the AAO template was carried out for the SEM sample (60 min, 100 °C, 85 % phosphoric acid).

TEM specimens were prepared in a standard way, with glueing, grinding, dimpling, and ion milling. The microscope was a JEOL 4010.<text>

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