Comparison of SiGe Virtual Substrates for the Fabrication of Strained Silicon-On-Insulator (sSOI) Using Wafer Bonding and Layer Transfer

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Different methods of preparing sSOI wafers have been analyzed. The initial virtual substrate wafers are characterized by a 17 - 20 nm thick strained silicon layer grown either on a thick relaxed SiGe layer on a graded buffer or on a thin SiGe buffer relaxed by He implantation.

Bonding and layer transfer experiments using different oxide layers proved that strained silicon layers are completely transferred if designed PE-CVD oxide layers were used. For both types of virtual substrates the oxide layers are deposited on top of the strained silicon and bonded to non-oxidized (blank) silicon wafers. A perfect layers transfer is obtained for virtual substrates having thick SiGe buffer layers (type A) even at 350°C, while annealing at 450 °C is required for substrates with thin SiGe buffer layers (type B). The lower annealing temperature for substrates of type A is caused by the lower activation energy for blistering. The hydrogen implantation is here into the SiGe. For type B substrates the hydrogen implantation is into the underlying Si requiring a higher temperature for layer splitting (higher activation energy for Si).

Introduction

The benefits of enhanced carrier mobilities in strained silicon (sSi) and reduced parasitic capacitances in silicon-on-insulator (SOI) substrates have recently been combined together in strained silicon-on-insulator (sSOI) technology [1]. The sSOI substrates are of immense importance for the new generations of CMOS technology. To obtain sSOI substrates the process of direct wafer bonding and layer transfer is presently used [2].

The sSi is grown on a relaxed SiGe virtual substrate and is then transferred to a Si handle wafer by direct wafer bonding. The Ge content in the SiGe alloy and the degree of plastic relaxation in the SiGe layer with respect to unstrained Si determines the degree of strain in sSi. The relaxation of the SiGe is mediated through misfit dislocations near the SiGe/Si interface. The misfit dislocations are connected to the free surface by dislocation segments threading through the layer. These threading dislocations (TDs) are penetrating not only through the SiGe but also through the sSi layer and may thereby deteriorate the device performance. The density of TDs is reduced by either slow compositional grading of the SiGe layer (10% Ge content grading per µm) [3,4] or by relaxation of a thin pseudomorphic SiGe layer (<500 nm) induced by hydrogen or helium implantation and subsequent annealing [5]. The latter type of substrates shows a much lower surface roughness (root mean square (RMS) < 1 nm) [5], while the graded virtual substrates show

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a cross-hatch pattern on the surface that gives rise to a RMS value > 1 nm [4]. In this case surface planarization is required prior to wafer bonding process.

**Experimental**

The SiGe layers with different Ge concentration were grown on silicon wafers (diameter 8 inch, (100) orientation) by chemical vapor deposition (CVD) methods. Two types of virtual substrates involving SiGe (type A and B) were used in this study. The as-grown substrates were investigated using cross section transmission electron microscopy (XTEM). The surface roughness of the as grown substrates (type A and B) was investigated by atomic force microscopy (AFM).

Both types of substrates were implanted with hydrogen using 130 keV H$_2^+$ ions with a dose of 3-5 $\cdot$ 10$^{16}$ cm$^{-2}$. Standard chemical cleaning (SC1 + SC2) followed by de-ionized (DI) water rinse was employed for all the wafers prior to bonding. The virtual substrates were then bonded to Si handle wafers in a Süss CL200. Different oxide layers were used in the interface, which were deposited before bonding either on the virtual substrate or on the Si handle wafer. In order to increase the bond strength and for layer splitting, the wafer pairs were annealed at moderate temperatures. The bond strength was estimated using the crack-opening method [6] immediately after the bonding at room temperature and after different annealing steps. The bonded interfaces were investigated (as bonded and after annealing) by infrared (IR) transmission microscopy.

**The Virtual Substrates**

Two types of virtual substrates were used in this study:

The first type (type A) consists of a 2 µm thick compositionally graded buffer layer, applied to grow a relaxed SiGe layer of the same thickness (Fig. 1). Relaxed SiGe layers were grown with different Ge content ranging from Si$_{0.83}$Ge$_{0.17}$ to Si$_{0.70}$Ge$_{0.30}$. On top of the relaxed SiGe layer a biaxially strained silicon (sSi) layer, about 17-20 nm thick was grown. The strain level of such a sSi layer varies from $\varepsilon = 0.64\%$ (using Si$_{0.83}$Ge$_{0.17}$) to $\varepsilon \approx 1.1\%$ (for Si$_{0.70}$Ge$_{0.30}$).

Depending on the growth process, the SiGe grading process may results in the formation of a cross-hatch pattern caused by strain fields from the misfit dislocations in the graded buffer. Measurements of the roughness by AFM result in a RMS value of about 2.7 nm for a 10x10 µm scan size.

The large surface micro-roughness inhibits wafer direct bonding. Several planarization steps were employed for some of the substrates. This includes deposition of various bonding layers and chemo-mechanical polishing (CMP).

The second type (type B) is represented by a pseudomorphic growth of a 150 nm thick Si$_{0.77}$Ge$_{0.23}$ layer. The SiGe layer is initially fully strained and the strain relaxation occurred by performing a He implantation using a dose of 7-10$^{15}$ cm$^{-2}$ and subsequent annealing in argon flow at 850°C for 10 min [7]. During this process a narrow defect band underneath the SiGe/Si substrate interface is generated. It provides a high density of dislocation loops as sources for misfit dislocations resulting in efficient strain relaxation during annealing. The dislocations propagate from the bottom of the relaxed SiGe towards the surface into the Si cap layer. On top of the Si$_{0.77}$Ge$_{0.23}$ layer a dislocation-free, strain adjusted Si$_{0.84}$Ge$_{0.16}$ layer was grown acting as substrate for the deposition of a strained silicon layer about 20 nm thick.
Figure 1: Typical XTEM images of the SiGe virtual substrates (type A). A relaxed SiGe layer (about 2 \( \mu \)m thick) is grown on top of a compositional graded layer.

Figure 2: Typical XTEM images of the SiGe virtual substrates (type B).

20 nm sSi (0.66% strain)

200 nm Si\(_{0.84}\)Ge\(_{0.16}\) strain adjusted

6 nm sSi seed layer

180 nm Si\(_{0.77}\)Ge\(_{0.23}\) partially relaxed

Misfit dislocation network

Figure 2: Typical XTEM images of the SiGe virtual substrates (type B).
**Wafer Bonding**

The low surface roughness of type B virtual substrates allows the bonding to oxidized Si substrates. The same bonding process is also applied to some of the type A substrates grown by an advanced SiGe deposition process [8]. The interface energy is about 0.3 J/m² after bonding at room temperature and corresponds to data measured for hydrophilic Si wafers. A subsequent annealing at 300°C for up to 10 hours increases the interface energy to about 1 J/m².

Type A substrates grown by the standard SiGe deposition process are characterized by a high surface roughness. RMS values of about 2.7 nm for a 10x10 µm scan size are typical. Therefore, in order to obtain a bondable surface the surface has to be planarized prior to bonding. A high density plasma (HDP) silicon oxide was deposited by chemical vapor deposition (CVD). The CVD deposition of HDP oxide was performed at low temperatures (< 400 °C) and the thickness of the HDP-CVD oxide is about 100 nm. Then, chemo-mechanical polishing (CMP) of the deposited layer was employed for short time and the RMS value was reduced up to approximately 0.7 nm. Due to the CVD process, gas molecules are incorporated into the deposited film and result in outgassing during subsequent annealing. It was reported that undesired outgassing induced by the annealing of the bonded pairs can be avoided by annealing of the deposited oxides prior to the bonding process, resulting in driving out of the surface water vapor or hydrocarbon species [9]. An outgassing process at 600°C in Argon atmosphere was performed for the deposited HDP-CVD oxide prior to wafer bonding.

In contrast, the second type of relaxed SiGe substrates has a lower surface micro-roughness. The RMS value is about 0.2 nm for a 10x10 µm scan size (AFM), and is sufficiently low to allow direct bonding without further surface planarization. Spontaneous bonding was observed when both types of substrates were brought in contact to the handle wafers at room temperature. Moreover, void free bonding interfaces are obtained immediately after the bonding process. Annealing of the bonded pairs was performed to increase the bond energy. Sequential annealing was used for the oxide deposited type A substrate. As shown in Fig. 3, a void free interface is observed after 5h annealing at 300°C. The interface energy after this first step is about 0.87 J/m². Further annealings for 2h at 500 °C result in an increase of the interface energy up to ~1 J/m². After similar post-bonding annealing of the type B substrate, several voids are detected at the bonding interface. The voids might be caused by the presence of some contaminants (hydrocarbons) at the bonded surfaces which may trap the existing gases during annealing.

Plasma enhanced (PE) CVD oxides were also used as intermediate layers for bonding. The CVD oxides were deposited onto the sSi/SiGe substrates. An outgassing process was also applied before bonding at 850°C for 30 min. Caused by the high surface roughness of PE-CVD layers an additional CMP process is required removing about 40 nm of the oxide layer thickness. Successful direct wafer bonding is achieved when the SiGe wafers, deposited with PE-CVD oxide, are bonded to non-oxidized (blank) Si wafers. As shown in the infrared transmission image of the bonded pair (Fig. 3c.) no bubbles or voids are present at the bonding interface also after annealing at moderate temperatures. Furthermore, interface energies of about 1.5 J/m² were measured even after annealings at 300°C.
Figure 3: Infrared microscope images of bonded wafer pairs. The SiGe virtual substrate (type A) was bonded to an oxidized Si handle wafer (a). Before bonding a HDP-CVD oxide (b) or PE-CVD oxide was deposited on the SiGe virtual substrate. Bonding to blank silicon wafers.

Layer Transfer

Layer transfer processes based on hydrogen implantation and wafer bonding were employed for the sSOI fabrication. SiGe virtual substrates of both types were implanted with H$_2^+$ at 135keV using doses of 3 to 5x10$^{16}$ cm$^{-2}$. The energy causes the peak of implantation induced damage to be about 0.6 µm deep according to simulations (SRIM 2003 [10]). For virtual substrates of the type A this corresponds to an implantation into the relaxed Si$_{1-x}$Ge$_x$ layer, while for type B substrates the peak of implantation induced damage is in the silicon substrate, about 100nm below the SiGe. Because the blistering kinetics is different for Si and SiGe, also a different behaviour of the layer splitting is suggested. For silicon an activation energy for blistering of $E_a = 0.47$ eV was reported for higher temperatures ($T > 500°C$) while $E_a = 2.5$ eV at lower temperatures under these conditions.
conditions [11]. The low activation energy at higher temperatures corresponds to the activation energy for atomic hydrogen diffusion, while the higher activation energy at lower temperatures is assumed to be the sum of two energies involving two combined mechanisms: hydrogen diffusion and dissociation of Si-H bonds. 

On the other hand, blistering experiments on SiGe layers proved an activation energy of $E_a = 0.38 \text{ eV}$ at $T > 400 \ ^\circ\text{C}$, while at lower temperatures ($300^\circ\text{C} < T < 400^\circ\text{C}$) the activation energy is only 1.2 eV [12]. 

For experiments both types of virtual substrates were used with different oxide layers in the interface. Two-step annealing sequences were used in all cases starting with an annealing at about $300^\circ\text{C}$ for longer times (20 h) followed by a shorter annealing step at temperatures between $350^\circ\text{C}$ to $450^\circ\text{C}$. The low-temperature annealing is used to increase the bonding strength, while the second annealing step introduces the layer splitting.

Figure 4a shows the optical image of a transferred layer. A type B virtual substrate with a HDP CVD oxide was applied. It is clearly shown that only parts of the layer are transferred. Analogous results were also obtained for type A virtual substrates if thermally grown oxides or HDP CVD layers were applied. There are 2 different reasons for the incomplete layer transfer: (i.) The formation of interface bubbles was observed especially for HDP CVD oxides during annealing at elevated temperatures. (ii.) Both types of virtual substrates deform during annealing in consequence of the different thermal expansion coefficients of the different SiGe layers and the underlying Si. The deformation results in a bow of the wafers which is higher for type A virtual substrates (by their thicker SiGe layers) than for type B wafers. If the interface energy is low debonding is obtained followed by blistering instead of layer splitting.

Furthermore, designed PE-CVD layers result in higher interface energies even at lower temperatures and can compensate the thermo-mechanical stresses in the layer system during annealing. This causes that strained silicon layers can completely transferred (Fig. 4b). A perfect layers transfer is obtained for virtual substrates of type A even at 350°C, while annealing at 450 °C is required for substrates of type B. The lower annealing temperature for substrates of type A is caused by the lower activation energy for blistering. The hydrogen implantation is here into the SiGe.

Figure 4: Optical images of wafers after the layer transfer using HDP CVD oxide (a) and a PE-CVD oxide (b) in the interface. Wafer diameter 200 mm.
Conclusions

Different methods of preparing sSOI wafers have been described. The initial virtual substrate wafers are characterized by a 17 - 20 nm thick strained silicon layer grown either on a thick relaxed SiGe layer on a graded buffer (type A) or on a thin SiGe buffer relaxed by He implantation (type B).

The different surface properties (surface roughness) allow wafer bonding without any pretreatments for virtual substrates of type B, while planarization steps (CMP or additional layer deposition) are required for virtual substrates of type A.

Bonding and layer transfer experiments using different oxide layers proved that strained silicon layers are completely transferred if designed PE-CVD oxide layers were used. For both types of virtual substrates the oxide layers are deposited on top of the strained silicon and bonded to non-oxidized (blank) silicon wafers.

A perfect layers transfer is obtained for virtual substrates of type A even at 350°C, while annealing at 450 °C is required for substrates of type B. The lower annealing temperature for substrates of type A is caused by the lower activation energy for blistering. The hydrogen implantation is here into the SiGe.

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References