Imaging of the lateral GOI-Defect distribution in Silicon MOS wafers with Lock-in IR-Thermography

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Yield and reliability of MOS devices are strongly affected by crystal originated particles (COPs) which may generate gate oxide integrity (GOI) defects. For the semiconductor industry it is highly desirable not only to measure the density, but also to image the lateral distribution of GOI-defects. A novel technique to image GOI defects across large gate areas has been developed. First, a low-ohmic bias pulse is used to break down nearly all GOI defects in a large-area MOS structure. Then a periodic bias of typically 2 V is applied and the local temperature variation caused by the leakage current through the broken GOI defects is imaged by lock-in IR-thermography. This technique has been used to image the GOI defect distribution across 8” Czochralski wafers. Various lateral variations of the defect distribution have been confirmed.

Keywords: GOI, gate oxide integrity defects, COP, IR-thermography, whole wafer mapping

1. Introduction

Crystal originated particles (COPs) are well known to strongly reduce the dielectric breakdown voltage of the insulating SiO₂ layer in MOS structures i.e. to cause gate oxide integrity (GOI) defects [1]. The density of GOI defects in a given wafer is one of the most important criteria for the semiconductor industry. So far, wafers have been characterized using electrical breakdown measurements on small capacitors (some mm²) evenly distributed across the wafer. That way the GOI defect density can be determined on a statistical basis, but only limited and poor information about the lateral defect distribution is gained. The knowledge of the defect distribution on the entire wafer area is important for a better understanding of defect formation during crystal growth and finally for the improvement of the Czochralski grown silicon material.

This contribution presents a new method for directly imaging broken GOI defects across large areas i.e. across whole wafers. The first step to image GOI defects is to apply a low-ohmic bias pulse to a whole wafer MOS structure in order to electrically break down preferably all GOI defects in the sample. In the second step the GOI defects are imaged using lock-in IR-thermography. The optimum pulse width to achieve breakdown of nearly all GOI defects and at the same time to keep the structural damage at the already broken defects low slightly depends on the defect density and is in the order of about 100 µs [2]. The use of a longer pulse width may result in high structural damage and consequently in the destruction or “self healing” [3] of some of the broken GOI
defects. “Self healed” or deactivated GOI defects are no longer electrically active, i.e., the conducting path through the oxide is destroyed and therefore they are no longer detectable with lock-in IR-thermography or by any electrical measurement. On the other hand, using a lower pulse width, the deposited energy may not be sufficient to break down all GOI defects. After the bias pulse has established an electrically conducting path through the oxide, a periodic voltage of typically 2 V and a frequency of 16 Hz is applied to the sample. The periodic current through the broken GOI defect causes via Joule heating a small temperature variation at the site of the defect. This temperature variation is detected by lock-in IR-thermography. A detailed description of the basic principle and of the used measurement system is given in [4, 5]. The achieved temperature resolution is about 10 µK for a 20 min measurement at a lateral resolution down to 5 µm. The determined defect densities show good agreement with electrical measurements. For the first time radial and large-scale variations of the GOI defect density could be directly visualized on whole wafer MOS structures.

2. Experimental

In this work we determine the GOI defect density and the radial GOI defect distribution of three different 8” Czochralski wafers. All investigated MOS samples had an oxide thickness of 25 nm and a 400 nm poly-silicon gate covering the whole wafer. Material 1 was specified with a high GOI defect density and material 2 and 3 had a low defect density. In principle whole wafers can be thermographically investigated, but for practical reasons the samples were cleaved into quarters. The poly-silicon gate was contacted using a 12 µm thick Ni-foil to ensure a homogeneous electrical field over the whole MOS structure. The sample was attached to a sample holder by placing a thin plastic film on top of the Ni-foil and the sample and applying a vacuum between the film and the sample holder. The local temperature variations at the site of the broken GOI defects were detected by the IR camera through the Ni- and the plastic foil. In order to have a higher IR emissivity the plastic film was painted black. Directly after cleaving the samples, thermograms of the quarter wafers were recorded. Material 1 was investigated by applying one low-ohmic bias pulse of 10 V and then one of 20 V corresponding to electrical fields of 4 MV/cm and 8 MV/cm for the oxide thickness of 25 nm. The used pulse width was 10 ms. Thermograms were recorded after each pulse. For material 2 and 3 we applied one 10 V and one 25 V pulse at a pulse width of 100 µs. Depending on the electrical breakdown field, A-mode (E < 4 MV/cm) or B-mode (4 MV/cm < E < 8 MV/cm) GOI defects were visualized.

3. Results and Discussion

Fig. 1 shows the recorded thermograms of the same quarter of material 1 after cleaving, after applying a 10 V and after a 20 V bias pulse of 10 ms. Directly after cleaving a thermographic signal was detected at the border of the wafer which is of no further interest for this investigation and is considered as an artifact. Only one GOI defect was observed in the inner area after cleaving. A bias pulse of 10 V did not cause more GOI defects to break down. Therefore the density of A-mode GOI defects is close to zero in this material. After applying a bias of 20 V the electrically activated
(electrically broken) B-mode GOI defects (right) were visualized. The B-mode GOI defect density was determined to be $28 \text{ cm}^{-2}$ and is homogeneous in the central wafer area. At a radius greater than about 8.5 cm the defect density is dramatically reduced.

Fig. 2 shows the thermograms of material 2 recorded after cleaving (left), after applying pulses of 10 V (middle) and 25 V (right) at a pulse width of 100 µs. Here all four quarters have been investigated and their images are reassembled. Directly after cleaving defects at the edge of the wafer are observed. Several A-mode GOI defects break down after applying a 10 V bias pulse. The picture on the right shows the broken GOI defects after a pulse of 25 V. The horizontal and the vertical line in this image is a signal from the cleaved edges i.e. an artifact and should not be observed if whole wafers are used. In this material the determined GOI defect density is about 0.36 cm$^{-2}$ and does not show a radial dependency. However, large-scale lateral variations in the defect distribution can be observed.

The images resulting from measurements on material 3 are shown in Fig 3. The current through the circumference of the wafer causes a signal at the lower edge of the wafer and of the contacting Ni-foil and is considered to be an artifact. In this material A-mode GOI defects detected after cleaving and after a bias pulse of 10 V were mainly located in one of the four samples, in the upper left quarter of the wafer. The A-mode GOI defects are distributed inhomogeneously. B-mode GOI defects break down mostly in the center of the wafer after applying a bias pulse of 25 V and 100 µs. The determined GOI defect density is $\sim 30 \text{ cm}^2$ in the center and $< 0.1 \text{ cm}^2$ outside the center. This is an example of a pronounced radial dependency of the GOI defect density.
4. Conclusion

In this work we have shown that lock-in IR-thermography allows to detect all electrically active GOI defects in a sample and therefore allows to investigate large MOS structures. We used this fast and reliable new method to visualize GOI defects and determined the defect density and distribution across quarters of wafers from three Czochralski silicon crystals grown with different growth conditions. Lock-in IR-thermography allows to investigate the quality of a given wafer material with respect to GOI defects and determine the useable wafer area. No complex and costly sample preparation like lithographic steps are needed. Lock-in IR-thermography is a powerful tool for the study of the defect distributions resulting from various growth conditions and can be utilized as a monitoring tool for the development of silicon crystals with very low GOI defect concentration.

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References