HIGH EFFICIENCY PERT CELLS ON N-TYPE SILICON SUBSTRATES

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ABSTRACTS

High minority carrier lifetimes of a few milliseconds have been demonstrated both on CZ and FZ n-type silicon substrates. It is particularly interesting that the phosphorus doped n-type CZ wafers give minority carrier lifetimes nearly as high as those from the best p-type FZ silicon materials. This gives a good potential for very high performance on n-type CZ substrates.

21.1% and 21.9% efficiencies are reported for PERT (passivated emitter, rear totally-diffused) cells fabricated on these n-type mono-crystalline CZ and FZ silicon substrates, respectively. High open-circuit voltages approaching 700 mV have been demonstrated by these cells. Unfortunately, a non-uniform emitter saturation current has caused low fill factors for these cells, which will be investigated in future research.

1. Introduction

World solar cell production has been rapidly increased by about 30% annually in the past a few years. Bulk crystalline silicon, including p-type boron doped Czochralski (CZ) single crystalline silicon and cast multicrystalline silicon, has been the work-horse for past world solar cell production with over 80% of cells presently fabricated on such materials [1].

However, solar cells fabricated on standard boron doped CZ silicon substrates have shown a reduced cell performance after being exposed to a light source and even after storage in the dark [2,3]. Such degradation effects recently have been investigated by many researchers. Schmidt and coworkers reported that such degradation results from the dopant boron which reacts with oxygen atoms under illumination [4]. The high oxygen density is a result from the standard CZ growth method. Hence, to reduce such degradation effects, one should try to avoid high levels of both boron and oxygen in the same wafer.

To avoid using boron dopant, high efficiency PERT cells had been previously fabricated on a variety of silicon substrates, resulted in very high cell performances, such as the 24.5% efficiency from a boron doped MCZ (magnetically confined Czochralski) [5], and the 21.9% efficiency from a gallium doped CZ substrate [6]. The low oxygen content in the MCZ materials and using gallium to replace boron in the CZ materials have both resulted in stable cell performance by reducing the possibility of reaction between boron and oxygen. In this paper, we have fabricated PERT cells on phosphorus doped n-type CZ and FZ substrates to avoid the boron-oxygen associated degradation problem.

2. PERT Cell Structure

The PERT cell structure (see Fig. 1) used for this n-type cell research is a reverse polarity structure compared to previously published PERT cells on p-type substrates [5,6]. A boron doped emitter is used to replace the previous phosphorus doped emitter. It has been commonly believed that the boron diffusion may cause excessive surface recombination compared to the phosphorus emitter. However, the improved performance for the previous PERT cells on p-type MCZ and CZ(Ga) substrates has demonstrated a high surface passivation quality at our boron diffused rear surface [5,6]. In the present work, we have relocated the previous rear boron passivation layer to the cell front surface to form the cell emitter. It is expected to give a similar cell performance to those PERT cells on p-type substrates.

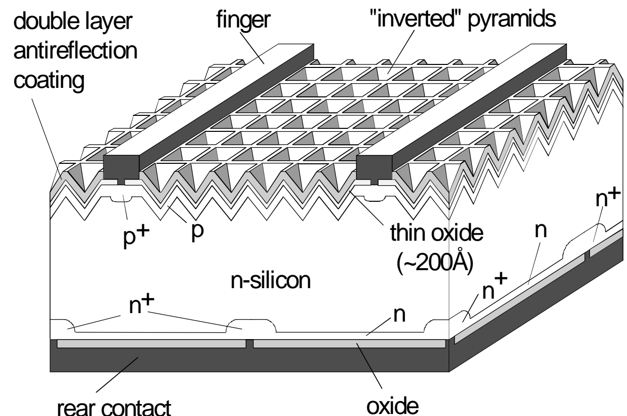

Fig. 1. PERT cell structure on n-type substrate.

Most of the cell processing steps are similar to our previously reported PERL cell processing [7]. N-type phosphorus doped, low resistivity, (100) orientation, CZ and FZ silicon wafers were used to fabricate these PERT cells. The front surface of the cells were etched into 'inverted pyramids' by KOH etch and by lithographically de-

fined SiO_2 masks. These inverted pyramids combined with the rear surface mirror form an excellent light trapping scheme, which traps the light between the front and rear surfaces for many passes [8]. The cell emitter is formed by BBr_3 diffusion, which results in low surface recombination velocities. The rear surface is also diffused by a light phosphorus diffusion to reduce the current crowding effect at the rear contact windows and hence reduce the cell series resistance. The front and rear surfaces of the cells are passivated by high quality TCA grown oxide. Such surfaces have extremely low surface recombination velocities. The small front and rear metal contact areas are further passivated with heavily diffused boron and phosphorus areas, respectively.

The front Ti/Pd contact metal was fabricated by a lift-off process. It was later thickened by electrolyte Ag plating. The rear contact metal, Al, was formed by thermal evaporation. An aluminium layer was also evaporated onto the cell front surface. After sintering in forming gas (4% hydrogen in argon), this aluminium layer is removed. This so-called 'alneal' process significantly reduces the surface recombination velocity. Finally, a ZnS/MgF_2 double layer antireflection coating was deposited onto the cell surface to further reduce cell reflection.

3. Advantages of N-Type CZ Silicon Substrates

The very first diffused silicon solar cells were made on n-type substrates in the 1950s. The solar cell industry changed to p-type substrates soon afterwards due to the higher resistance of this polarity to space radiation, at a time when the only application for those cells was for space vehicles. This p-type substrate tradition continues to the present terrestrial application era, although it might not be the best choice for terrestrial cells. Hence, it is now of great interest to reinvestigate the possibility to use n-type substrates again. In fact, the phosphorus doped n-type silicon has many advantages over the standard boron doped silicon substrates. These advantages are listed as followings:

a. Avoidance of boron-oxygen degradation
b. Higher minority carrier lifetimes
c. Ease of thermal oxide passivation
d. Higher conductivity for given substrate doping
e. Better concentrator cell performance
f. Reduced current non-linearity

N-type substrates usually have higher minority carrier lifetimes than p-type substrates. The measured minority carrier lifetimes from p-type and n-type wafers have been published previously [3]. However, only a TCA grown silicon dioxide was used to passivate the surface of undiffused wafers in those experiments. In the present work, the n-type wafer surfaces were diffused with phosphorus at both surfaces, and then passivated by a TCA grown oxide. A phosphorus diffused surface is expected to improve surface passivation, and hence increase the measured effective carrier lifetime. The effective carrier lifetime was measured by the PCD (photo-conductance decay) method with a Leo Giken carrier lifetime tester.

Figure 2 shows the effective carrier lifetime measurement results. Different processing and storage conditions are listed in Fig. 2, where the notation FG350 represents sintering in forming gas (FG) at 350°C and nCz1.3 represents 1.3 Ω·cm n-type CZ substrates. All FG sintering and alneal (aluminium anneal) processes were carried out for 30 minutes. It can be seen in Fig. 2 that all the tested cells have effective carrier lifetimes greater than 1 millisecond (ms). Even with the lower minority carrier mobility values reported in n-type compared to p-type, which gave effective carrier lifetime in the range of 0.5 to 2 ms [3], this results in similar or larger minority diffusion lengths for n-type over p-type substrates. Among the SEH n-type CZ substrates, the 5.5 Ω-cm substrate gives the highest effective carrier lifetime of 5 ms.

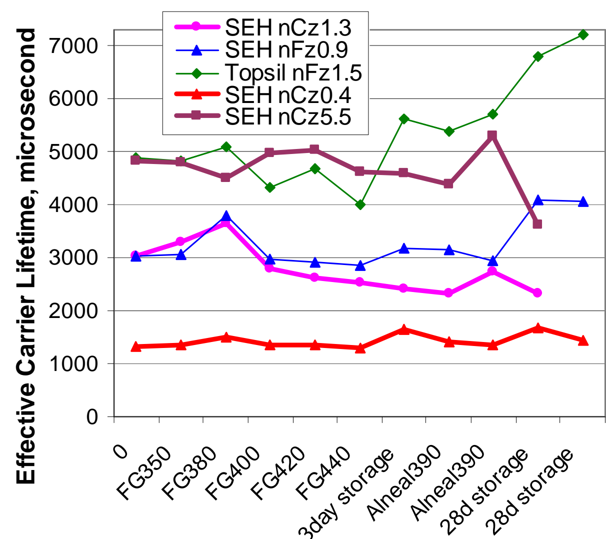

Fig. 2. Measured effective carrier lifetime under different processing and storage conditions. Both surfaces of the wafers were diffused with phosphorus.

These measured minority carrier lifetimes are significantly higher than those previously measured in boron doped p-type FZ silicon substrates [3]. Hence, it gives a potential for cells on such n-type CZ materials to match the performance levels which have been demonstrated by cells on boron doped FZ silicon substrates.

4. Cell Performance

Table 1 lists the performance of the PERT cells on CZ and FZ n-type silicon substrates, tested at Sandia National Laboratories under the standard $100 mW/cm^2$ AM1.5 global spectrum, at 25°C. The CZ cell, Wn08-1d, has demonstrated 21.1% energy conversion efficiency. This is the highest efficiency ever reported for a cell made on an n-type CZ silicon substrate. As far as we are aware, the next best result on an n-type CZ silicon substrate is from HIT cells, which used amorphous silicon heterojunctions to passivate the silicon surfaces [9].

With 0.4 Ω-cm substrate resistivity, Wn08-1d, has given a high open-circuit voltage (V_{oc}) of 687 mV, which is

in the vicinity of values for our previously reported p-type FZ cells. Future work will attempt to reduce the area of the boron emitter to further reduce the emitter saturation current density. These n-type CZ cells also give relatively high short-circuit current densities, J_{sc}. The best previous PERT cell on a 5.3 Ω-cm p-type gallium doped CZ substrate had J_{sc} = 41.0 mA/cm^2, while having V_{oc} = 680 mV and 21.9% efficiency [3]. Although the 5.5 Ω-cm n-type cell, Wn08-5a, had a lower efficiency, it had a slightly higher J_{sc} than the best counterpart p-type CZ(Ga) cell.

Table 1. The performance of 4 cm^2 PERT cells on n-type CZ and FZ silicon substrates, tested at Sandia National Laboratories under the standard 100 mW/cm^2 AM1.5 global spectrum, at 25°C.

Cell ID	Material	Resistivity	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Effic. (%)
Wn08-1d	CZ	0.4	687	40.3	75.9	21.1
Wn08-3c	CZ	1.3	679	40.4	76.6	21.0
Wn08-5a	CZ	5.5	679	41.2	75.5	21.1
Wn10-5d	FZ	0.9	695	41.1	76.5	21.9

Table 1 also shows the performance of a PERT cell on a FZ silicon substrate. It has demonstrated a 21.9% energy conversion efficiency. The n-type FZ cells have generally higher open-circuit voltages and similar short-circuit current densities and fill factors to n-type CZ cells.

Unfortunately, all the PERT cells on n-type CZ and FZ substrates have very low fill factors of 75-77%. An analysis below will show that these low fill factors are not caused by resistive losses.

Interestingly, the PERT cells on n-type CZ substrates have shown stable performances, although rather heavily boron doped emitters were used in these cells. Since oxygen levels in these emitters are also high, this might have been expected to lead to the formation of active defects in the emitter under illumination. The reduced carrier diffusion length in the emitter may still be significantly longer than the emitter thickness. Hence the minority carriers generated in the emitter region have a collection probability close to unity, even after degradation.

5. Cell Characterisation

Figure 3 shows as bold lines the measured dark I-V (low current values) and J_{sc}-V_{oc} curves (high current values), as well as their local ideality factors m. The curves are connected together where they overlap in order to keep them free from resistive losses. A striking feature is the hump shortly below 0.6 V, responsible for the above-mentioned low fill factors. This hump depends only weakly on the base doping level, if at all. It is an extraordinary smooth hump, i.e. the ideality factor rises steadily from 0.2 V, where it is near 1, towards higher voltages, where it reaches m≈1.7. Such behaviour can not be explained by resistive losses. By means of numerical modeling, we have examined a few possible reasons for it, as outlined in the following.

Since the observed hump is nearly identical for all three wafer resistivities, it may be caused by the emitter. Introducing an uneven emitter (boron) diffusion with regions of high sheet resistivity, the simulations reproduce the experimental I-V curves well (thin line in Fig. 3).

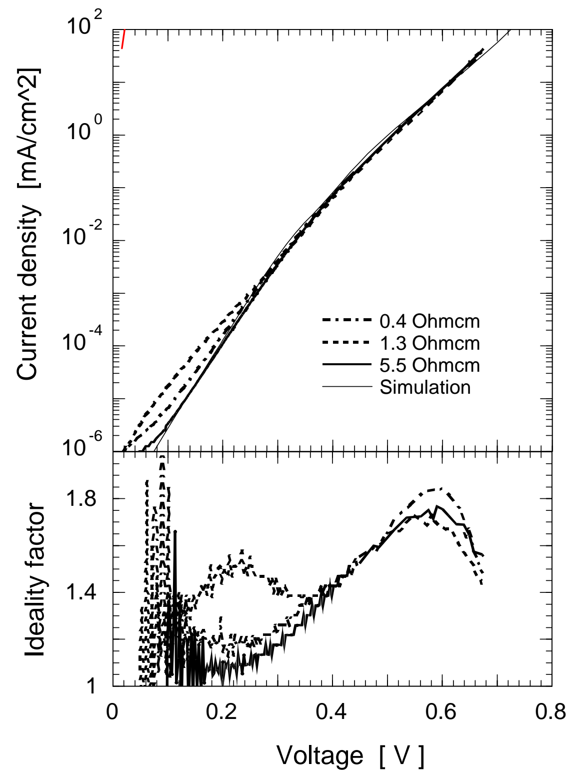

Fig. 3. Experimental I-V curves and ideality factors (bold lines) and simulation (thin line).

Instead of having regions with a high sheet resistivity, the emitter may be homogeneous but exhibit a strong boron depletion near its surface. In such a case, the surface recombination losses may dominate the I-V curve despite a good surface passivation because both carrier types have similar densities, making SRH recombination very effective. The hump arises as the surface switches from low to high injection conditions in this model, as discussed for bulk regions below. Boron depletion near the surface has been observed previously in boron doped wafers [10], however not to the extent necessary to produce the hump observed here. The depletion may be more severe if boron is diffused into the wafer material instead of being added to the melt.

To confirm the homogeneity of the saturation current of the boron emitter, the heating effect of the cell dark current is tested with a Lock-in Thermography method performed at Max Planck Institute of Microstructure Physics, Halle, Germany (see Fig. 4). The details of this method are discussed by a separate paper in this conference [11]. In Fig. 4, the bright areas are a few milli-Kelvins hotter than the rest darker areas, under a forward bias current of 39.9 mA for the 4 cm^2 cell.

It is seen that a large part of the boron emitter is hotter (brighter) than the rest of the cell, possibly due to higher saturation current. A few leakage current hot points at the bottom left corner and also in the left and the top areas are seen in Fig. 4. These shunted areas increase the dark forward current and hence also contribute to reduced cell fill factors.

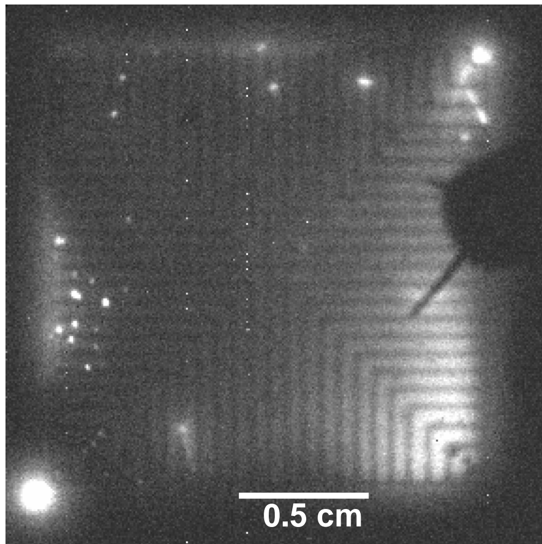

Fig. 4. Thermography image of FZ n-type cell, Wn10-5d, at 0.67V, 39.9 mA, 24 Hz, with scale 0 to 1 mK.

Hence, we need to improve the quality of the boron doped emitter. We can also reduce the emitter area coverage over the cell front surface to reduce the emitter saturation current in future experiments.

6. Conclusions

This paper has demonstrated the potential for using the n-type CZ silicon substrates to fabricate high efficiency solar cells. The advantages of using n-type substrates for solar cells are discussed in detail. A low fill factor problem is observed for PERT cells both on CZ and FZ n-type substrates. Metal contact and bulk resistance seem not to be the cause of this problem. Numerical analysis and thermography both show that a possible cause for this problem is a non-uniform boron doped emitter. This can be improved by further optimisation of the emitter boron diffusion process. A future improvement may be achieved by reducing the emitter saturation current density with partial emitter coverage.

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