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Fabrication of Metal-Ferroelectric-Silicon Structure by Layer Transfer via Wafer Bonding

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The paper presents fabrication of metal-ferroelectric-silicon structures by a layer transfer process via direct wafer bonding. PZT and SBT ferroelectric thin films were deposited by chemical solution deposition on 3″ Pt–coated silicon wafers and subsequently crystallised by conventional thermal annealing. The ferroelectric films were polished by standard chemical mechanical polishing in order to decrease the surface roughness under 1 nm RMS and to achieve the bonding conditions. The ferroelectric/Si wafers were directly bonded to silicon wafers using a microcleanroom set up and subsequently annealed in air at temperatures lower than 500°C. MFS heterostructures were electrically characterised by capacitance-voltage and current-voltage measurements. The direct wafer bonding prevents formation of low permittivity layer between Si and the ferroelectric film and improves significantly the interface trap density.

Keywords: Metal-ferroelectric-silicon structures, direct wafer bonding, ferroelectric thin film

INTRODUCTION

In recent years, a major effort has been made to integrate ferroelectric materials into semiconductor technology. Ferroelectric capacitors have already been integrated into silicon CMOS circuits to produce commercial nonvolatile memories [1–3]. Due to its simplicity and non-destructive read out, the idea of a ferroelectric field effect transistor (FeFET) as a memory cell remains a goal for ferroelectric–Si integration although realization attempts were not successful so far. High temperature, which is basically required to obtain high quality ferroelectric thin films, has to be avoided to give undesirable interface reactions at semiconductor–ferroelectric interface. One way to avoid the reactions is to grow a buffer layer acting as diffusion barrier between Si and ferroelectric film. The present paper

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shows an alternative approach to build ferroelectric–semiconductor devices by direct wafer bonding (DWB) of ferroelectric films to a silicon wafer [2]. This method requires thermal treatment after bonding at lower temperatures, usually in the range of 200°C to 500°C. After this annealing the Si surface remains totally undamaged and the native Si oxide layer acts like a very thin buffer layer [4, 5]. All interactions between the ferroelectric layer and Si happen only in very thin layer, which is usually in range of few nm. In this way it is possible to avoid presence of e.g. strong PbO diffusion and strong interface roughening are observed after high temperature film preparation of PZT [5]. This paper shows electrical investigations on metal-ferroelectric-silicon (MFS) heterostructures prepared by with different films.

EXPERIMENTAL

Two different ferroelectric thin films—$Pb(Zr_{0.60}Ti_{0.40})O_3$ (PZT) and $SrBi_2Ta_2O_3$ (SBT) were obtained by chemical solution deposition. Films were deposited onto Si or Pt-coated Si wafers by spin coating method and pyrolized at 300°C for 5 min. The deposition procedure was repeated three times in order to increased the film thickness to about 450 nm. The amorphous films were etched at the rim of the wafer in order to eliminate the inherent thickness non-uniformity resulting from the spinning process. Finally, the films were crystallised by conventional thermal annealing in air for 1 h at 650–800°C.

In order to achieve the bonding conditions and to improve the surface roughness, the ferroelectric films were polished by a standard chemical mechanical polishing using a Logitech polishing machine and a Chemcloth polishing pad [6, 7]. The polishing slurry was composed of syton, water and glycerol (4:4:1). After polishing, the wafers were ultrasonically cleaned for 2 hours in deionized water to remove any Syton particles. The film surface morphology was investigated by atomic force microscopy (AFM) (D5000, Digital Instruments) and the roughness was measured before and after polishing.

Finally the wafers were bonded under hydrophilic conditions to a plain silicon wafer (covered with native silicon oxide), by the standard direct wafer bonding technique in micro-cleanroom set up [7]. The bonding quality was examined using an infrared video camera and an IR light source. In order to increase the surface energy at the bonded interface obtained at room temperature, the wafer pairs were annealed 12–24 hours at temperatures 450–500°C.

The MFS structures with a ferroelectric–Si bonded interface were obtained by polishing down the handling wafer and subsequently etching away

in KOH at 80°C. The top electrodes were deposited on top of the ferroelectric film by gold evaporation through a metallic mask. The electrical properties of the MFS structure with the ferroelectric-semiconductor bonded interface were investigated by measuring the capacitance-voltage (C-V) and current-voltage (I-V) characteristics. C-V curves were taken at 10 kHz using a Hewlett–Packard HP4192 impedance analyzer and I-V characteristics were measured using a Keithley 6517 electrometer.

RESULTS AND DISCUSSION

The as grown PZT film has a surface morphology as is shown in Fig. 1. The root mean square (RMS) roughness value, computed from this image, is about 30 nm. After polishing, the roughness decreases drastically up to 0.8 nm (see Fig. 1), which fulfil the bonding requirements. The wafers with the ferroelectric films were bonded to plain silicon wafers by standard direct wafer bonding. After successful room temperature bonding (see Fig. 2) the interface energy of the bonded interface is increased by a thermal treatment at a temperature low enough to prevent interdiffusion. The surface energy increases typically to about 1.5 J/ m^2 after a 24 h thermal treatment at 450°C. After this processing the Si surface remains totally undamaged as previous TEM analyses showed [4, 5]. The native silicon oxide layer in the MFS structures acts like a very thin buffer layer between Si and ferroelectric film.

The electrical characterisations of MFS heterostructures with bonded interfaces have been carried out by measuring C-V and I-V characteristics.

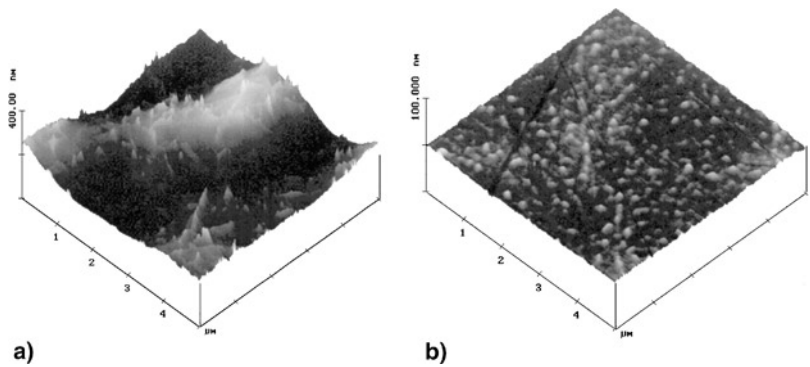

Figure 1. Surface morphology of PZT film a) after crystallisation at 650°C and b) after polishing.

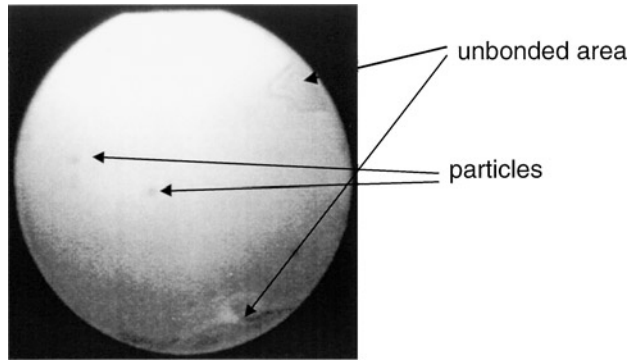

Figure 2. Infrared transmission photograph of a PZT/Si wafer bonded to a Si wafer. The bonded area appears bright and the dark area indicates an incompletely bonded area.

The results were compared with the properties of reacted interface obtained by a direct deposition of PZT by chemical solution deposition and SBT by pulsed laser deposition. The C-V measurements of PZT hererostructure, presented on Fig. 3, shows a clockwise hysteresis, which reveals the ferroelectric

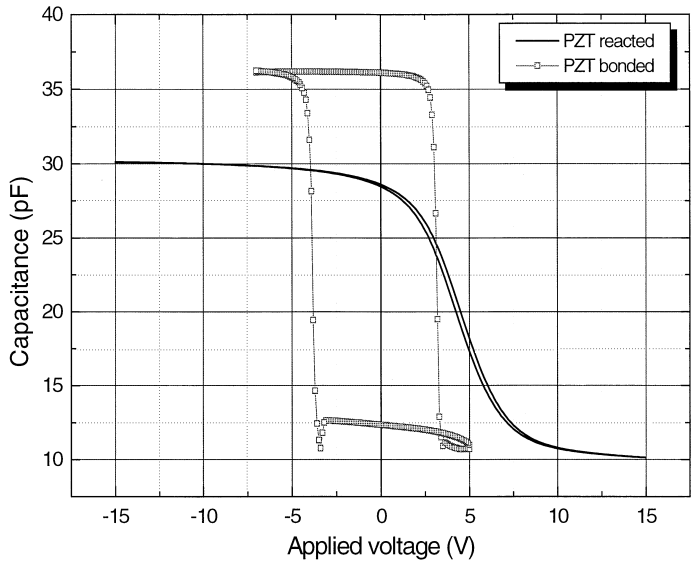

Figure 3. C-V characteristics of PZT/Si reacted and bonded interface.

properties of the gate oxide. The analysis of these characteristics show that the values of permittivity are higher for bonded structures compared with MFS structures obtained by direct deposition of ferroelectric films onto silicon. In case of SBT/Si structure the effective permitivitty is 32.3 for film prepared by PLD and 88 for the bonded structure. Using the DWB approach the formation of a low-k interface layer can be avoided.

The interface trap densities (D_{it}) were determined by using the conductance loss G_{it}/ω or the equivalent parallel conductance G_p/ω. This loss due to the interface traps was determined by measuring the admittance of the MFS diodes biased in depletion [8, 9]. The peak value of the frequency dependence of capacitance conveys the main information on interface trap density at a specific gate-to-bulk voltage (V_{gb}) corresponding to a depletion regime. From this dependence the interface trap density distribution over the band gap energy near the midgap can be derived. The dependence of the trap densities on difference between gate-to-bulk voltage V_{gb} and flat-band voltage V_{FB} for PZT/Si and SBT/Si reacted and bonded interfaces are given in Fig. 4. It can readily be seen that the trap densities are higher for reacted interfaces then for the bonded ones. The higher tap density of the PZT/Si reacted interface can be related to the high reactivity of Pb-based ferroelectrics during high temperature annealing, in which PbO diffuses into Si and reacts to form glassy $PbSiO_x$.

The bonding interfaces shows the trap density distribution with midgap value about 4×10^{11} $cm^{-2}\,eV^{-1}$. This value is, however, about ten times

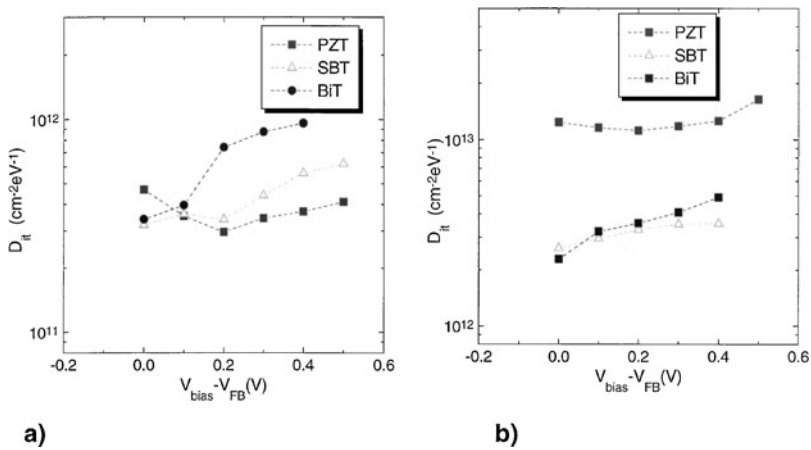

Figure 4. Interface trap density distribution of a) reacted and b) bonded ferroelectric/Si.

higher than that of standard SiO_2-based gate oxides [10]. This relatively high trap density may be caused by well know low quality of the native SiO_2/Si interface and can probably be improved by applying a standard cleaning-oxidising process before bonding.

CONCLUSION

Electrical measurements reveal a large difference for the MFS structure depending on whether interface is generated by bonding or by direct deposition. The direct wafer bonding and layer transfer process gives better quality ferroelectric/Si interfaces avoiding formation of low permittivity (low-k) layer between Si and decrease of interface trap density by one order of magnitude.

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