High epitaxial quality Y$_2$O$_3$ high-$\kappa$ dielectric on vicinal Si(001) surfaces

G. Apostolopoulos, a) G. Vellianitis, and A. Dimoulas
Molecular-Beam Epitaxy Laboratory, Institute of Materials Science, National Center for Scientific Research “DEMOKritos,” 153 10 Ag. Paraskevi Attikis, Greece

M. Alexe and R. Scholz
Max-Planck-Institut für Mikrostrukturphysik, Weinberg 2, D-06120 Halle, Germany

M. Fanciulli, D. T. Dekadjevi, and C. Wiemer
Istituto Nazionale per la Fisica della Materia, Laboratorio MDM, Via C. Olivetti 2, 20041 Agrate Brianza (MI), Italy

(Received 28 June 2002; accepted 16 September 2002)

Thin films of Y$_2$O$_3$ were grown by molecular-beam epitaxy on silicon aiming at material with adequate crystal quality for use as high-$\kappa$ gate replacements in future transistors. It was found that Y$_2$O$_3$ grows in single-crystalline form on 4° misoriented Si(001), due to an in-plane alignment of ⟨110⟩$_{Y_2O_3}$ to the silicon dimer direction. The Y$_2$O$_3$ layers exhibit a low degree of mosaicity, a small proportion of twinning and sharp interfaces. This represents a significant improvement compared to material grown on exact silicon surfaces. © 2002 American Institute of Physics.

[DOI: 10.1063/1.1519727]

The growth of very thin dielectric layers on semiconductor surfaces has attracted much attention during the last few years, primarily due to the aggressive down-scaling of complementary metal–oxide semiconductor (CMOS) devices. Although advances in lithography have significantly reduced the transistor physical gate length, scaling is limited by the gate dielectric material. The required thickness of less than 2 nm for SiO$_2$, the standard gate dielectric used so far as high leakage currents, thickness nonuniformity, and dopant penetration. A remedy to this issue is the replacement of SiO$_2$ with a suitable new dielectric of higher permittivity $\kappa$. This allows maintaining the gate dielectric physical thickness sufficiently large ($>$4 nm) so as to combine reliable, low power operation with high-frequency performance.

Although research and development worldwide has focused on amorphous HfO$_2$ and ZrO$_2$ by atomic layer chemical vapor deposition, a suitable high-$\kappa$ candidate has not been identified yet. A more radical approach, pursued by a number of research groups, is epitaxial growth of metal–oxide dielectrics by molecular-beam epitaxy (MBE). Epitaxial metal oxides could offer advantages such as higher dielectric constant and better control of interfaces. On the other hand, at the high temperatures needed in CMOS processes most of the amorphous high-$\kappa$ oxides tend to become polycrystalline, with grain boundaries and thus high leakage. This could be prevented if the material is prepared in single-crystalline form as in the epitaxial case, which could be advantageous. However, epitaxial oxides also present problems, and there is still no clear evidence of superior characteristics compared to amorphous dielectrics. In view of this, the present work aims at exploring ways to improve the structural quality of the epitaxial dielectric yttrium oxide (Y$_2$O$_3$) candidate.

Yttrium oxide is attractive as a gate oxide for silicon transistors due to its $\kappa$ value ($\kappa\sim$14–18), its predicted thermodynamic stability, the relatively high conduction band offset ($\sim$2.3 eV), and the lattice commensurability with Si (a$_{Y_2O_3}$=2a$_{Si}$). Like many other rare-earth oxides having a fluoritelike crystal structure, it grows heteroepitaxially on Si(001) in an unfavorable orientation such that Y$_2$O$_3$(110)||Si(001). This gives rise to a complex twin microstructure, which is a drawback for using Y$_2$O$_3$ as a gate dielectric due to the potential electrical leakage through the domain boundaries. Recently, there have been reports mainly for Gd$_2$O$_3$, indicating that twinning may be avoided by growing on misoriented substrates. There is also evidence, mainly by reflection high-energy electron diffraction (RHEED), that Y$_2$O$_3$ shows the same behavior, but a systematic and quantified investigation is still lacking.

In this letter, we report results on high-quality epitaxial Y$_2$O$_3$ grown by MBE on vicinal Si(001) and subsequently characterized by RHEED, high-resolution transmission electron microscopy (HRTEM) and x-ray diffraction (XRD). In addition, we compared these results with the ones obtained from epitaxy on exact substrates. Using 4° misoriented substrates we have obtained single-crystalline Y$_2$O$_3$ layers with a very small amount of twinning and low values of mosaicity, among the best reported in the literature. The double-stepped surface of 4° misoriented Si(001) comprising of Si dimers parallel to the step edges, imposes an alignment of ⟨110⟩$_{Y_2O_3}$ along these edges over the entire wafer. Our results indicate the existence of a preferred orientation of the dielectric crystal with respect to the dimers of the reconstructed Si surface.

The Y$_2$O$_3$ layers were grown in a MBE system under ultrahigh vacuum conditions. 2 in. Si(001) wafers, exact, 2°, and 4° misoriented towards [110], were cleaned with standard chemical methods and inserted into the growth chamber. The native oxide was removed by heating to 770 °C for
1 min under a Si flux of 0.5 Å/s. RHEED showed a (2 × 1) reconstruction, indicating a clean starting Si surface. A 200 nm thick undoped Si buffer layer was grown at a substrate temperature of 650°C. This allowed us to obtain a good quality starting surface since the primary purpose of this work is to study the growth and structural properties of the film and its interface with silicon. However, the undoped (resistive) buffer layer prevented electrical characterization by standard metal–insulator–semiconductor capacitor testing. Y2O3 was evaporated at a rate of 0.5 Å/s by means of an electron gun onto the Si substrate held at 450°C and was subsequently annealed for 20 min at the same temperature.

Y2O3 has the cubic bixbyite Mn2O3 structure with a lattice constant of 10.6 Å. It has a lattice mismatch of 2.4% with respect to Si, if one considers two silicon unit cells. However, as previously mentioned, the material grows with the Y2O3(110)[Si(001)] orientation, for reasons that have not been clarified yet. A possible explanation may be given considering the electrical neutrality of the crystalline Y2O3 layer is indeed reconstructed, indicating a clean starting Si surface. A typical structure of an Y2O3 layer grown on exact Si(001) under the same conditions is shown in Fig. 2(a) and b for comparison. The HRTEM image shows the coexistence of two twinned domains, labeled A and B, in the Y2O3 layer. One of them has [110]Y2O3[110]Si and the other [001]Y2O3[110]Si. Note that in contrast to the diffraction pattern in Fig. 2(a), this sample shows two adjacent Y2O3 spots, (004) and (222) as shown in the inset, characteristic of the presence of the twin structure.

In order to quantify the amount of twinning in the Y2O3 films we performed x-ray reciprocal space mapping analysis. Figure 3 shows maps of the Y2O3(222) diffraction peak from the layer grown on the misoriented silicon wafer at two different φ positions. The higher intensity map in Fig. 3(a) originates from domains having the orientation deduced above by RHEED. However, we could also detect a weak

![Image](https://example.com/image.jpg)
contribution from 90° rotated domains at an azimuth $\phi = 90°$ [Fig. 3(b)]. By comparing the integrated intensity of the two peaks, it can be estimated that the volume fraction of rotated domains in the layer is $\sim 5\%$. Note that the volume fraction determined by reciprocal space analysis has also been confirmed by pole figure analysis. The small amount of rotated domains could not be detected by cross section TEM, since only a small fraction of the sample volume can be probed by this technique. Although we are not able to estimate the average domain boundary free area due to the lack of information on the twinned domains lateral dimensions and distribution, the extremely low fraction (5%) of twinned domains suggests that the device yield may not be significantly affected.

Similar analysis for the $2°$ misoriented sample showed a 35% volume fraction of rotated domains, while in the exact sample the volume fraction of each domain is 50%. The mosaicity of the $Y_2O_3$ layers was determined from XRD rocking curves. Figure 4 shows the results for a sample grown on a 4° misoriented Si(001) substrate. The mosaicity deduced from this measurement is about 1.31°, which is one of the best values reported in the literature and compares favorably with the value of 2° reported for Gd$_2$O$_3$ on 4° misoriented Si(001). Similar measurements for $Y_2O_3$ grown on 2° misoriented and exact wafers (not shown here) exhibited a mosaicity of 1.46° and 2.31°, respectively, clearly indicating that the epitaxial quality has been improved using vicinal substrates.

From the results reported herein, it may be inferred that the misorientation of the Si substrate plays a significant role in the nucleation of the $Y_2O_3$ layers. The structure of the misoriented Si(001) surface has been studied extensively by a number of experimental techniques. It is known that at small misorientation angles $\phi_m$ the Si(001) surface consists of both $(2 \times 1)$ and rotated “$(1 \times 2)$” reconstruction domains. The Si dimer axis direction is 90° rotated in the latter case. At higher $\phi_m$ $\approx 4°$, dimers are always aligned parallel to the step edges, thus the portion of rotated $(1 \times 2)$ domains is drastically reduced. Considering the in-plane epitaxial orientation of $Y_2O_3$ on our $\phi_m = 4°$ samples, we may conclude that $(110)_{Y_2O_3}$ is preferentially oriented parallel to the surface steps and thus to the Si dimers. The observed 5% volume fraction of rotated $Y_2O_3$ domains could be due to the presence of small amounts of rotated $(1 \times 2)$ surface domains, where $Y_2O_3$ also tries to fulfill its preferential orientation with respect to the silicon dimers. Indeed, from the data given in reference, a 5% $(1 \times 2)$ surface coverage may be estimated for $\phi_m = 4°$. At $\phi_m = 2°$ and 0°, the $(1 \times 2)$ surface coverage increases to 25% and 50%, respectively, and the volume fraction of the rotated $Y_2O_3$ domains follows quite closely this behavior. Nevertheless, evidence is still lacking as to the origin of this preferential alignment of $(110)_{Y_2O_3}$ to the silicon dimers, and further work is required to clarify this point.

From a technological point of view, the use of misoriented substrates may require modifications in the standard semiconductor processing techniques, although it may also be beneficial for the oxide reliability. Nevertheless, this would be one of the many issues related to the compatibility of high-$\kappa$ materials (epitaxial or amorphous) with CMOS technology. Regarding epitaxial materials, one possible problem could be the enhanced Boron penetration due to channeling effects during implantation. However, using a non-standard CMOS process sequence, the junction could be formed using a sacrificial SiO$_2$ gate prior to gate dielectric deposition, in which case dopant penetration is not an issue.

In conclusion we have shown that the growth of $Y_2O_3$ is substantially improved using vicinal Si(001) substrates. Twining in the epilayer depends on the $(2 \times 1)$ and $(1 \times 2)$ “disorder” of the Si surface reconstruction. In the case of $\phi_m = 4°$ $(110)$ misorientation, the highly ordered $(2 \times 1)$ double stepped surface offers an excellent template for the growth of high-quality single crystalline $Y_2O_3$ material with the $(110)_{Y_2O_3}$ aligned in-plane along the silicon dimer direction. The layers are characterized by a small value of the mosaicity of about 1.3° and a very small percentage (5%) of twinned regions. This reduces significantly the amount of domain boundaries which is expected to minimize the potential source of electrical leakage in future scaled high-$\kappa$ transistors.

This work was funded by the European project IST-28495-INVEST “Integration of very high-$\kappa$ dielectrics with Silicon CMOS technology.”