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Si/GaAs heterostructures fabricated by direct wafer bonding

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ABSTRACT

Si/GaAs heterostructures were obtained by a low temperature direct wafer bonding (DWB) method which uses spin-on glass (SOG) intermediate layers. The use of intermediate SOG layers allows the fabrication of Si/GaAs heterostructures at processing temperatures lower than 200°C. The achieved bonding energy permits thinning down to a few microns of Si and GaAs wafers, respectively, using grinding procedures followed by chemical mechanical polishing (CMP). After thinning, the heterostructures sustained annealing temperatures of 450°C without damaging of the bonded interface. The above bonding procedure was successfully applied for bonding GaAs wafers to Si wafers with structured surfaces. A technology was developed based on this bonding method for producing universal GaAs-on-Si or Si-on-GaAs substrates.

INTRODUCTION

Monolithic integration of compound semiconductors into silicon technology would result in new applications in optoelectronics, microwave electronics, and high temperature electronics. A specific interest is focused on the fabrication of Si/III-V compound semiconductor heterostructures. The combination of high performance III-V compound semiconductor optoelectronic devices with the charge handling functionality of modern silicon circuitry would enable the fabrication of monolithically integrated optical interconnects which will increase considerably the speed of data processing and transmission [1]. Silicon is also an ideal supporting material for GaAs and other III-V compound semiconductors due to its superior mechanical strength, low weight, and high thermal conductivity [2].

Classical thin film deposition techniques like low temperature epitaxy, metalorganic chemical vapour deposition or molecular beam epitaxy were used for the fabrication of GaAs layers on Si substrates. Compared to bulk GaAs, GaAs thin films on Si substrate suffer from two major problems: i) the presence of high dislocation densities due to the 4.1 % lattice mismatch between Si and GaAs (typical $10^6 \div 10^8$ cm^{-2}, instead of 10^3 cm^{-2}, which is desired for device fabrication), and ii) the biaxial tensile stress generated in the plane of GaAs film during cooling from the deposition temperature due to the thermal mismatch (thermal expansion coefficient - TEC - of GaAs is almost double than the TEC for Si) [3].

Direct wafer bonding (DWB) can be a valuable solution for solving the lattice mismatch problem as long as this technique impose conditions only to the flatness, microroughness and the cleanliness of the surfaces and is not depending on the crystalline properties of the two materials. Thermal mismatch remains also an issue for DWB but in the last years low temperature bonding techniques were developed (vacuum bonding [4], plasma activation methods [5, 6], bonding with

intermediate layers [7, 8]) which can be applied to diminish the stress thermally generated at the interface during annealing.

This paper presents a novel low temperature DWB method which has been successfully applied to fabricate Si/GaAs heterostructures.

EXPERIMENTAL

Three bonding procedures were evaluated: i) hydrophilic bonding of GaAs and Si followed by annealing up to 300°C, ii) O_2 plasma activation of surfaces before bonding followed by annealing up to 300°C, and iii) bonding *via* a spin-on glass (SOG) intermediate layer.

(100) oriented semiinsulating GaAs wafers, 100 mm diameter, and (100) oriented p-type Si wafers, 100 mm diameter were used for experiments. The Si wafers were cleaned before bonding using the standard chemical cleaning procedure with RCA 1 ($NH_4OH:H_2O_2:H_2O$ = 1:1:5) and RCA 2 ($HCl:H_2O_2:H_2O$ = 1:1:5) solutions. The GaAs wafers were first rinsed with deionized water for particle removal. Then the wafers were cleaned in a $NH_4OH:H_2O$ = 1:20 solution for the hydrophilic bonding and bonding *via* SOG layers. For oxygen plasma activation, the GaAs wafers were only rinsed in deionized water. The bonding procedures were performed in a class 10 cleanroom.

For the plasma activation of the surfaces the two wafers were introduced into an O_2 plasma reactor for 5 minutes (oxygen pressure – 1.5 torr, radio frequency power – 600 W) and then bonded using the procedure described above.

Finally, the bonding *via SOG* was applied. SOG layers were deposited by a spin-on technique onto the Si wafers. The thickness of the SOG layer was measured using a profiler after a step was etched into the layer. The deposited wafers were bonded with GaAs wafers and then annealed at low temperatures.

The bonded interface was investigated using infrared (IR) transmission, scanning acoustic microscopy (SAM) and transmission electron microscopy (TEM). The surface energy was measured with the crack opening method and tensile testing. The tensile test was performed on small samples cut from the bonded wafer pairs (6 x 6 mm^2). IR spectroscopy was used to study the chemistry of the glass intermediate layer. The fracture surfaces resulted after the samples brake during the tensile test were investigated with atomic force microscopy (AFM) and scanning electron microscopy (SEM).

RESULTS AND DISCUSSION

First, GaAs wafers were hydrophilic bonded with Si wafers. The surface energy at RT was about 20 mJ/m^2 and increased to about 80 mJ/m^2 after annealing at 300°C in a time range from 10 to 30 hours. The interactions mediating the adhesion at RT are weak and allow the wafers to separate during heating. The process is reversible and the wafers bond again during cooling stage. An oxygen plasma activation of the surfaces increases the surface energy at RT to about 80 mJ/m^2. By annealing the bonded wafer pairs in nitrogen at temperatures up to 350°C, debonding occurs due to the high stress developed at the interface and sometimes the GaAs wafers shatter. The use of an intermediate SOG layer was recently proposed as a low temperature method for GaAs/Si bonding [9].

A 350 nm thick layer was deposited onto Si wafers by spinning of a commercially available silicate SOG precursor. The resulted films were baked in air at temperatures up to 180°C. The SOG coated wafers were RT bonded with GaAs wafers using the standard bonding procedure. The surface energy at RT was about 0.4 J/m^2, almost four times higher than the surface energy in case of Si/Si hydrophilic bonding. This very high surface energy can be a result of the chemistry at the SOG-GaAs interface, which is very different from the usual silicon-silicon bonding. Infrared spectroscopy measurements presented in figure 1 revealed the existence of CH_3 radicals in the SOG films baked at temperatures below 200°C.

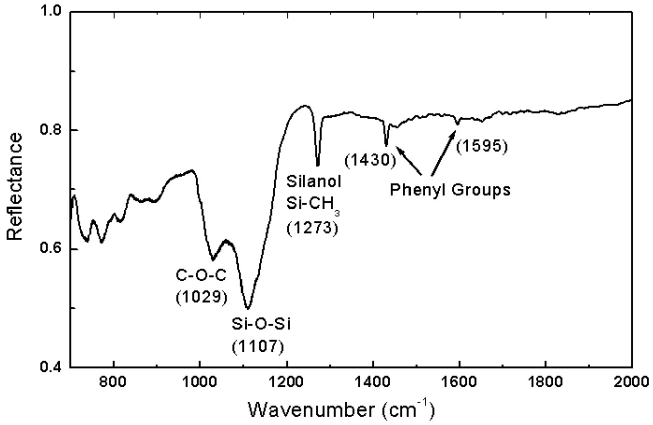


Figure 1. Infrared reflection spectrum of an SOG layer baked at 150°C.

The residual organic radicals remained from the solvent in the SOG layer can easily hydrolyze with the water molecules adsorbed at the Si surface and create strong covalent bonds. Even after a baking procedure at 150°C for 5 minutes the SOG surface contains also silanol groups, which may generate adhesion at RT due to their ability to form bonds with molecules from the other surface directly or *via* water molecules.

After RT bonding the samples were annealed at temperatures in the range 200°C –300°C for different tims. IR transmission images and acoustic micrographs (figure 2) showed good quality interfaces after the thermal annealing.

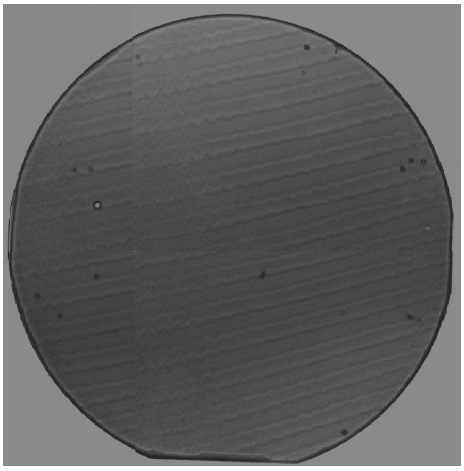
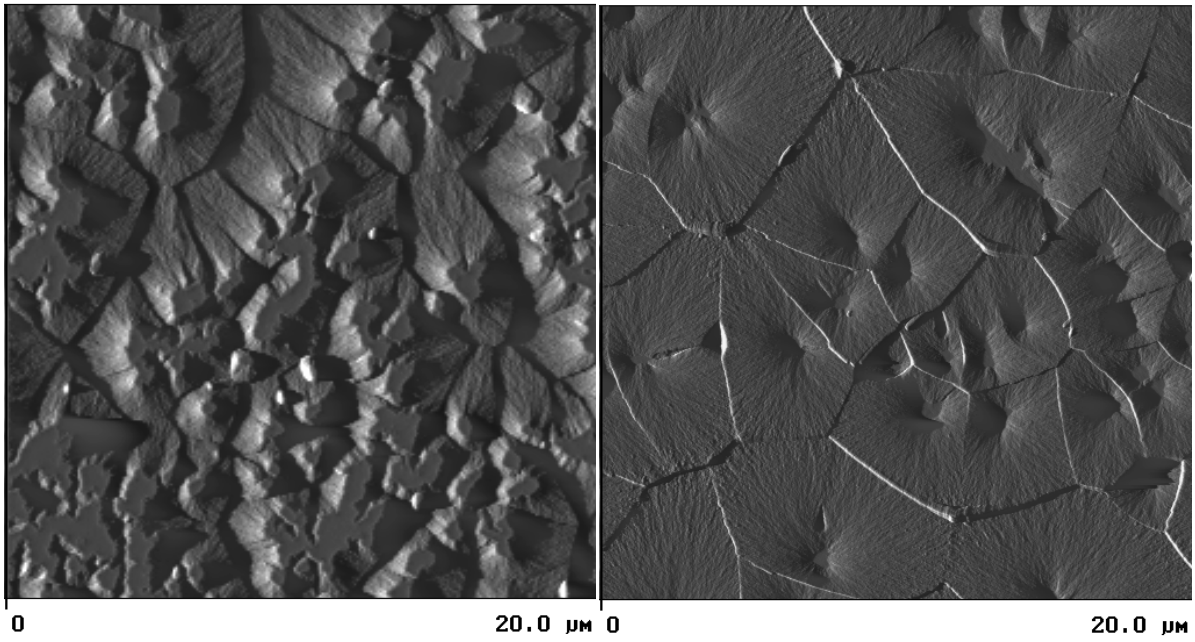


Figure 2. Acoustic micrograph of a bonded Si/GaAs wafers pair.
Grey contrast shows the bonded interface, white spots represent unbonded areas.

The surface energy increased up to 2 J/m^2 after an annealing at 200°C for 10 hours. Further increasing of the annealing temperature does not produce a significant increase of the surface energy. Some of the Si/GaAs bonded wafer pairs were heated up to higher temperatures. At about 280°C the wafers were debonding and shattered.

Samples of 6 x 6 mm^2 were cut from the bonded pairs annealed at 200°C and submitted to tensile stress testing. The samples cracked at values of about 22 MPa. AFM (figure 3) and SEM (not presented here) investigation of the resulted broken surfaces revealed that the SOG film brakes during the tensile test. This demonstrates the suitability of the SOG layer as "adhesion layer".



(a.) (b.)

Figure 3. AFM images of (a.)- Si wafer, and (b.)-GaAs wafer surfaces resulted after tensile esting.

The bow of the bonded wafer pairs was measured *in situ* during annealing. At 200°C a high bow of about 500 µm was measured. The bow is decreasing to zero during cooling of the bonded pair down to RT. For repeated heating-cooling cycles with the same bonded pair it was observed that the bow follows the same path at heating as well as cooling, showing no hysteresis. SAM investigations revealed that the bonded interface remained intact during this test, no voids being generated. This elastic behavior of the SOG layer compensates the high stress developed at the interface due to the thermal mismatch.

In order to prove that the surface energy achieved after annealing at 200°C is high enough to allow the subsequent processing of the as obtained Si/GaAs heterostructures, one of the bonded wafers was thinned by grinding followed by chemical mechanical polishing (CMP). The thinning procedure was applied to GaAs (thinned down to about 10 µm) as well as to Si (thinned down to about 5 µm). After thinning, the GaAs-on-Si and Si-on-GaAs resulting wafers were heated at 450°C. Further investigations revealed that the bonded interface remained unchanged, no voids

being generated. The thinning of one of the bonding partners diminish the thermally induced stress which causes the debonding of the thick wafers.

APPLICATIONS OF BONDING WITH SOG INTERMEDIATE LAYERS

The SOG bonding procedure described above was developed as an industrial technology for producing universal GaAs-on-Si substrates. By this method, substrates having different insulator or GaAs layer thickness can be easily produced for wafer diameter up to 150 mm.

The same bonding approach was applied for bonding GaAs epitaxial wafers with CMOS Si wafers. In this case, the main problem encountered is the planarization of the structured CMOS wafer. SOG is widely used for planarization in microelectronics industry but is not efficient when large area structures are present on the surface (in this case, about 5 x 5 mm^2 with 1.5 µm depth). Figure 4 shows the profile of a structure measured with a profiler.

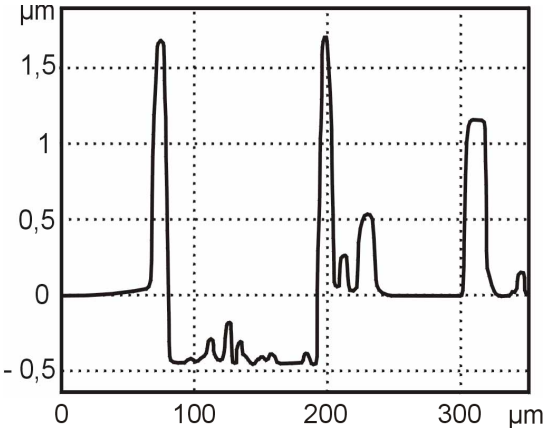


Figure 4. Profile of a structure on the CMOS Si wafer surface.

An efficient planarization method was the deposition of a 1 µm thick Si_3N_4 layer on top of the structured wafer, followed by the deposition of a 2 µm thick SiO_2 layer. The oxide was then planarized using CMP. The nitride layer acts as a polish stop layer. After the CMP planarization an SOG layer was deposited for a final planarization and as a bonding intermediate layer. The planarized wafers were bonded with GaAs wafers as described. The low processing temperature prevents both damage of the structures and decomposition of the compound semiconductor. Using the above described process, GaAs multiple quantum wells (MQW) were transferred to a standard CMOS Si wafer. MQW multilayer structures were grown on GaAs substrate and then bonded to a planarized CMOS Si wafer. Finally the GaAs substrate was back etched and the multilayer structures were patterned.

CONCLUSIONS

A new method was successfully applied for Si/GaAs heterostructures fabrication: bonding through an intermediate spin-on glass layer. The main advantages of SOG use are: i) SOG is an

electronically clean material, which does not produce contamination of Si or GaAS and ii) SOG can be easily deposited at RT using an usual spinner.

The surface energy for Si/GaAs pairs bonded with this procedure is about 0.4 J/m^2 for RT bonded wafers and increases to about 2 J/m^2 for annealing at 200°C for 10 hours.

The thermally induced stress develops a high bow at 200°C (about 500 µm) and leads to debonding at temperatures close to 300°C.

Si-on-GaAs (6 µm Si top layer thickness) and GaAs-on-Si (10 µm GaAs top layer thickness) wafers were fabricated by thinning one of the bonded wafers by grinding and CMP. The as obtained wafers sustain temperatures of 450°C without damaging of the bonded interface.

This bonding process was applied for bonding GaAs epitaxial wafers to CMOS Si wafers. The CMOS Si wafer was planarized by deposition of a polish stop Si_3N_4 layer and a SiO_2 layer followed by CMP. The electrical interconnections between the CMOS structures and the top GaAs layer can be realized by etching vias into the insulator layer.

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