Measurement of interface trap states in metal–ferroelectric–silicon heterostructures

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Interface trap density distributions within Si for metal–bismuth titanate–silicon capacitors fabricated by chemical solution deposition were investigated. The interface trap density was measured by a conductance technique at room temperature and a value in the order of $10^{11} - 10^{12} \text{eV}^{-1} \text{cm}^{-2}$ was found depending on the ferroelectric crystallization temperature. An increase in the annealing temperature results in an increase in the interface trap density.

In recent years, extensive research and development work has been carried out in order to achieve integration of ferroelectric materials into semiconductor technology. Ferroelectric capacitors have already been integrated into silicon-based integrated circuits to produce commercial nonvolatile electric capacitors. Ferroelectric memories are the ferroelectric field-effect transistor (FET) which is, in fact, a metal–oxide–semiconductor field effect transistor (MOSFET) with a ferroelectric oxide as gate. The information is read by sensing the FET channel current which depends on the polarization state of the ferroelectric gate. Therefore, the read process is nondestructive and since typically a cell is rewritten only $10^8$ times but is read over $10^{10}$ times, the fatigue problem would be less important. Due to its simplicity and nondestructive readout, the ferroelectric field effect transistor as a memory cell remains a goal for ferroelectric–Si integration although realization attempts were so far not successful. The main problem in ferroelectric FET devices is that the information vanishes after a certain time, i.e., the retention time is low, being in the range of $10^{4}$ s. Only one work, however not confirmed, reported a retention time of more than 1 y.

As had been pointed out from the very beginning, the main cause for retention time failure was the existence of a very high trap density at the semiconductor–ferroelectric interface which drastically affects the semiconductor surface properties and therefore alters the transistor characteristics. It is known that four general categories of charged defects are significant contributors to MOS degradation, namely: oxide-trap charge, interface trap charge, fixed-oxide charge, and mobile ionic charge. However, oxide- and interface-trap charges remain topics of great importance to MOS long-term reliability. For the metal–ferroelectric–semiconductor (MFS) case the bulk trap density in the ferroelectric oxide is in the range $10^{19} - 10^{21} \text{cm}^{-3}$ which gives $\sim 10^{14} \text{cm}^{-2}$ surface trap density at the ferroelectric–silicon interface. Trap density and activation energies were measured for ferroelectric oxides by different methods including thermally stimulated currents and dc leakage currents. The defects which generate these trap levels are situated physically within the oxide and often are mistaken for interface traps/states in the MFS case. These traps in the oxide can communicate on relatively slow time scales with the underlying Si and have been associated with hysteresis in $C-V$ measurements and $1/f$ noise in MOS devices.

So far, for the MFS structures no distinction was made between the traps in the ferroelectric oxide and the traps in the semiconductor and, moreover, no direct measurement was carried out in order to extract the silicon trap properties at the silicon–ferroelectric interface. In the present work interface trap density distributions are measured for MFS structures fabricated by chemical solution deposition (CSD) of Bi$_4$Ti$_3$O$_{12}$ onto Si and crystallized at different temperatures.

MFS heterostructures were prepared by Bi$_4$Ti$_3$O$_{12}$ (BiT) thin films deposition onto $p$-type, (100) oriented Si wafers. The BiT films were deposited using a CSD method described in detail elsewhere. Briefly, a stock solution was prepared using Bi–diethylhexanoate and Ti isopropylate as metal precursors and xylene as solvent. The substrates were spin coated at 3000 rpm for 35 s and the resulting metalorganic films were pyrolyzed at 350 °C for 5 min. The whole procedure was repeated three times in order to increase the film thickness to about 450 nm. Finally, the BiT films were crystallized by conventional thermal annealing in air for 30 min at different temperatures in the range 500–650 °C. The silicon substrates were commercial grade, (100) oriented, $p$-type, having a doping level of about $3 \times 10^{15} \text{cm}^{-3}$ and were not submitted to any cleaning procedure before BiT coating. The MFS capacitors were obtained by electroding the BiT–Si heterostructures. The top electrodes (gates), having 0.5 mm$^2$ area, were deposited onto BiT film by gold evaporation through a metallic mask. The back electrodes were obtained by aluminum evaporation onto the free Si back surface. Prior to Al deposition, the native Si oxide was removed by a standard HF etching.

The capacitance–voltage characteristics ($C-V$) and charge–voltage ($Q-V$) characteristics were measured at room temperature in a light tight probe station. Small-signal admittance measurements at frequencies ranging from 100 Hz to 1 MHz were carried out using an HP4192A impedance analyzer with an oscillator signal of 0.1 V. The $Q-V$ mea-
measurements used a Keithley 6517 electrometer/voltage source. The sweep rate during high frequency measurements was 0.1 V/s, whereas the ramp rate for quasistatic measurements was 0.01 V/s. The interface trap densities were extracted from the admittance measurements using the conductance method.6,14,15

The interface trap density \( D_{it} \) was determined by using the conductance loss \( G_{it} / \omega \) or the equivalent parallel conductance loss \( G_{p} / \omega \). This loss due to the interface states traps was determined by the measured admittance of the MFS diode biased in depletion. The equivalent parallel conductance loss is given by

\[
\frac{G_p}{\omega} = \frac{C_{it}}{2 \omega \tau_p} \ln[1 + (\omega \tau_p)^2],
\]

(1)

where \( C_{it} \) is the interface trap capacitance, \( \tau_p \) is the interface trap response time, and \( \omega \) is the angular frequency. The equivalent parallel conductance is not equal to the measured parallel conductance, \( G_m \). \( G_p \) is extracted from the measured admittance, \( Y_m = G_m + j \omega C_m \), \( C_m \) being the measured capacitance, by subtracting the reactance of the ferroelectric oxide capacitance. The equivalent parallel conductance loss is given by

\[
\frac{G_p}{\omega} = \omega C_{ox}^2 G_m \left[ G_m^2 + \omega^2 (C_{ox} - C_m)^2 \right].
\]

(2)

Figure 1 shows the dependence of \( G_p / \omega \) on frequency at different gate-to-bulk voltages. The interface trap density was calculated from

\[
D_{it} = \left( \frac{G_p}{\omega} \right)_{f_p} \left[ q f_D(\sigma_A) \right]^{-1},
\]

(3)

where \( f_p \) is the frequency corresponding to the peak value of \( G_p / \omega \), \( f_D \) is universal function depending on the standard deviation of band bending, \( \sigma_A \), \( A \) is the capacitor area. The \( f_D(\sigma_A) \) values determined from our samples were about 0.31–0.38. Figure 2 shows the interface trap density as a function of the gate-to-bulk voltage for different anneals of the BiT film. Usually, \( D_{it} \) is given as a distribution over the band gap energy near the midgap and not as a function of the gate-to-bulk voltage, \( V_{gb} \). In the case of MOS devices with linear dielectric as oxide gate, the first approximation theory fits quite well and the silicon surface potential, \( \Psi_{sc} \), is linear dependent on the gate-to-bulk voltage, \( V_{gb} \). In the MFS case, \( \Psi_{sc} \) does not only show a non-linear dependence on \( V_{gb} \), but it also has two different values depending on the polarization state.16

Usually, for MOS capacitors, the \( \Psi_{sc} \) value is determined using the quasistatic capacitance–voltage characteristics obtained from the \( Q-V \) method.6 The measurement is done using a bias-independent capacitor, \( C_i \), connected in series with the MOS sample, sweeping the gate-to-bulk voltage and measuring the signal across the \( C_i \). The result for a MFS structure is depicted in Fig. 3 and one can notice that it resembles quite well a ferroelectric hysteresis loop. In fact,
the $Q-V$ measurement setup as is described in Ref. 6 is a Sawyer–Tower setup working at very low frequencies (0.1 Hz or lower). The influence of the silicon capacitance, which is important only in depletion and weak inversion, can be observed around $V_{gb} = 0$ V when a double inflection in the loop becomes visible. Outside this region, silicon is either in accumulation or in inversion and can be considered as an electrode. The result is that the series capacitor $C_i$ will integrate, beside the displaced current due to the linear part of the ferroelectric oxide, the current generated by polarization switching, and the leakage current. The leakage current, which for the usual ferroelectrics is several orders of magnitude larger than the leakage current in SiO$_2$, is one of the most important disturbing factors at low sweeping frequencies. For these reasons the low-frequency $C-V$ curve cannot be computed simply by numerical differentiation of the $Q-V$ curve, a model considering the switching charge and leakage current (and its field dependence) should be developed. The only result which can be extracted from $Q-V$ measurements is the silicon band bending.

The above discussion indicates that simple models developed for the MOS characterization cannot be directly used in the case of MFS. But even taking into account all these difficulties, we consider that the conductance method can be applied on MFS structures with a major restriction in determination of $\Psi_{sc}$. Any other effects concerning silicon as series resistance and bulk trap loss can be extracted using the described methods. In fact, the most disturbing and not quantified effect which can give large errors in the results is the slow retention behavior. This effect, which is a slow modification of the MFS capacitance during the measurement, cannot be related to any measurement parameterlike frequency or applied bias.

The interface trap density for the BiT–Si system, as depicted in Fig. 2, is in the $10^{11}–10^{12}$ eV$^{-1}$ cm$^{-1}$ range and the distribution in the band gap for almost all samples is increasing as the energy approaches the midgap. One important fact is that an increase in the annealing temperature results in an increase in the interface trap densities, $D_{it}$. This is in agreement with the hypothesis that a reaction between Si and ferroelectric film is developing during the crystallization annealing. This reaction not only damages the ferroelectric film, but also introduces defects in the Si and the interface, increasing in such a way the trap concentration at the Si surface. Having in mind that the actual MOS technology requires an interface trap density in the $10^{10}$ eV$^{-1}$ cm$^{-1}$ range, a trap density of $10^{12}$ eV$^{-1}$ cm$^{-1}$, which is obtained for the highest annealing temperatures, makes the Si inadequate for further processing of devices like a field effect transistor.

In conclusion, we have shown that the conductance method can be applied for MFS structures in order to measure the interface trap densities in Si. The trap densities in Si are several orders of magnitudes lower than those reported for ferroelectric materials, but still are larger than those needed for real field effect devices. It remains to be shown that the use of buffer layers or direct wafer bonding for MFS structures will result in a significant decrease in interface trap density. It also remains unsolved whereas real field effect devices are more disturbed by the traps in the ferroelectric than by the interface traps in Si.

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