ELSEVIER

Physica B 308–310 (2001) 1205–1208

PHYSICA B

www.elsevier.com/locate/physb

Interface defects in integrated hybrid semiconductors by wafer bonding

P. Kopperschmidt*, St. Senz, R. Scholz

Max-Planck-Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany

Abstract

The integration of materials by wafer bonding offers novel device fabrication for applications in micromechanics, microelectronics, and optoelectronics. Two mirror-polished surfaces are brought into intimate contact by adhesive forces regardless of their crystallography, crystalline orientation and lattice mismatch. Followed by a thermal treatment at several hundred degrees centigrade, the interface energy of the material combination is increased to energies of covalent interatomic bonds. Attempts to break the bond lead to fracturing of the materials. In particular, thermomechanic stress in dissimilar material combinations may result in bending, gliding and cracking of the bonded wafers during annealing. The bonding interface of various hybrid semiconductor materials was studied by transmission electron microscopy. Occasionally, microscopic imperfections at the bonding interface were found in Si/Si, Si/GaAs, GaAs/GaAs, GaAs/Al_2O_3, GaAs/InP and moreover Al_2O_3/Al_2O_3 bonded wafer pairs. The imperfections were identified as voids, negative crystals, and oxide-containing precipitates ranging from 5 to 20 nm in diameter. Microscopic defects at the bonding interface in integrated bulk materials do not affect the mechanical and electrical properties of the device very much. However, in bonding of thin films the defects or precipitates may thread through the thin film, if the diameter of the precipitate surpasses the thickness of the film. These pinholes-containing thin films have a high leakage current, low electrical breakthrough and crystallographic disorder. Epitaxy of material on a pinholes containing, disordered surface results on deposition of bicystalline grains. In between the grains tilt grain boundaries were observed raising from the bonding interface. Bonding related defects at the interface can be avoided by alternative bonding techniques like UHV wafer bonding and low temperature wafer bonding.

PACS: 82.30.Rs; 61.72.Qq; 68.35.Fx

Keywords: Semiconductor wafer bonding; Interface defects; TEM micrographs

1. Introduction

The wafer bonding technique has been established in research and development in terms of integrating various materials [1]. Two mirror-polished wafers are brought into intimate surface contact at room temperature and adhere by van der Vaals forces. To receive high bonding strength, the wafer pair must be annealed at elevated temperatures. Two major problems arise for conventional wafer bonding including a high-temperature annealing step. During heating of wafer pairs containing different materials, thermomechanical stress is introduced into the material leading to bending in analogy to bi-metals. If the stress is sufficiently high, either the two wafers separate by breaking the bonds at the interface or one wafer will fracture [2]. The second problem of the high-temperature procedure arises from the occurrence of voids, crystalline grains and precipitates at the bonding interface. These imperfections are revealed in many materials combinations, e.g. silicon/silicon, GaAs/silicon, GaAs/GaAs, Al_2O_3/GaAs, Al_2O_3/Al_2O_3 and GaAs/InP [3–7].

*Corresponding author. Fax: +49-345-5511223.
E-mail address: kopper@mpi-halle.de (P. Kopperschmidt).

0921-4526/01/$ - see front matter
PII: S0921-4526(01)00943-7

If two bulk materials are joined together, microscopic interface defects may not have a disturbing effect on the mechanical and electrical properties of the device, if the density of the cavities is small. In thin films, however, where the size of the interface defect surpasses the thickness of the thin layer, the surface is decorated with trenches and pinholes and the associated device structure may have preventable properties [2]. In electronic applications these pinholes will lead to high leakage currents and a low electrical breakthrough across the interface. Incidentally, a twist in between a thin pinhole-containing crystalline layer and a single crystalline substrate has some interesting morphological features, as a template for bi-crystalline structures or selected area growing films.

By cross sectional and plan-view transmission electron microscopy (TEM) bonding interfaces of various materials combination are inspected and briefly discussed in the following.

2. Silicon/silicon bonding interfaces

In Czochralski grown silicon (CZ-Si) oxygen is incorporated in silicon with a concentration close to the solubility at the silicon melting point [8]. Oxide precipitates are formed at sufficient temperatures by diffusion processes. Large precipitates grow at the expense of smaller precipitates to reduce the surface energies. Grain boundaries often reduce the velocity of the diffusion and are therefore attractive nucleation centers for precipitates and void formations. In Fig. 1 a high-resolution TEM cross section is presented at the twist-grain boundary between two (0 0 1) bulk CZ-Si wafers after Ref [4]. The wafers are bonded hydrophobically with an intentional misorientation of 12°. Similar results were observed in thin silicon layer bonded to silicon substrates by Chen et al. They identified the defects as SiC containing precipitates [3].

3. GaAs/GaAs bonding interfaces

In GaAs/GaAs wafer bonding at 580°C in hydrogen atmospheres two types of interface defects were found. A representative TEM cross section is given in Fig. 2. In addition to amorphous precipitates, well-ordered grains of not-identified crystalline phases were observed at the bonding interface. These grains may be probably formed at elevated temperatures by lowering the surface energy at the boundary between two bonded surfaces with twist and miscut. In thin GaAs films with thickness of a few nm bonded to GaAs substrates, interface defects or cavities occasionally thread through the thin layer [7,9]. The decorated surface of the substrate may play an important role in the strain relaxation during lattice mismatched heteroepitaxy on the so-called 'compliant substrates'. Fig. 3 shows a TEM micrograph pointing out the interface of a twist bonded thin GaAs film bonded to GaAs substrate with a cavity defect. While removing the sacrificial layer AlAs, the interface cavities partly open to the surface of the transferred film. Patriarche et al., recently reported on GaAs/GaAs bonding interfaces containing a high density of a regular network of unbonded cavities [9]. Since their thin GaAs layer has a thickness of 20 nm, the cavities do not thread through the thin layer.

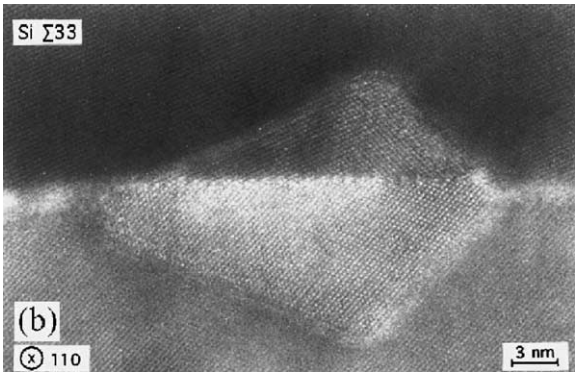

Fig. 1. High-resolution TEM cross-section at the bonding interface of two slightly twisted (0 0 1) silicon wafers. The SiO_2 containing precipitate consists of two tilted pyramids (after Ref. [4]).

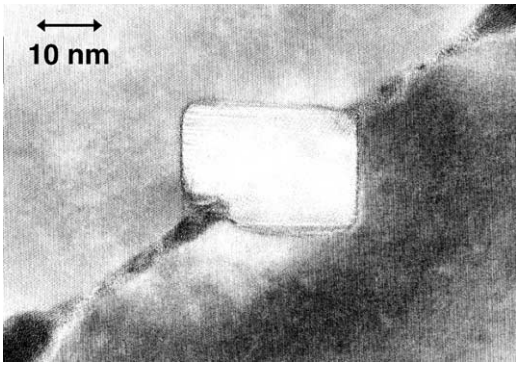

Fig. 2. Crystalline grain at the GaAs/GaAs bonding interface revealed by cross sectional TEM inspection. The crystallographic planes of the grain boundaries are close to [1 1 1]. Due to a small surface miscut of the (0 0 1) GaAs wafers, the grain is not exactly square-shaped.

4. Si/GaAs bonding interfaces

Since the thermal expansion coefficient of GaAs is nearly twice that of Si, thermomechanical stress cannot

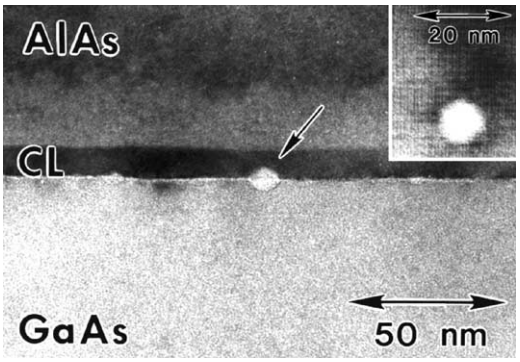

Fig. 3. Cross sectional (large picture) and plan-view (small picture) TEM micrograph of a defect at the interface of a thin GaAs layer bonded to a GaAs substrate. The GaAs thin film is denoted with CL. After removing the sacrificial AlAs layer, the GaAs layer is transferred to the GaAs substrate. If the size of the defect surpasses the thickness of the thin layer, pinholes or trenches are introduced into the thin layer after transfer.

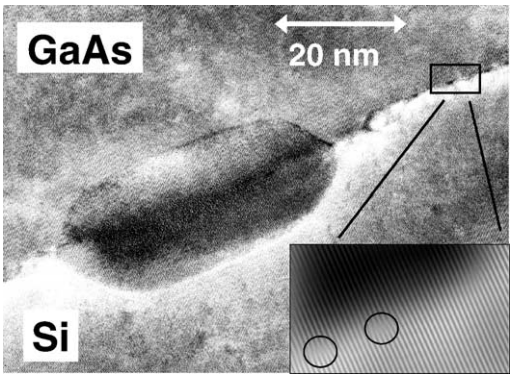

Fig. 4. Defect in Si/GaAs wafer bonding revealed by cross sectional TEM investigation. A Fourier-filtered image shows the bonding interface in detail. Due to the lattice misfit of 4.1%, extra (1 0 0) Si lattice planes are introduced (marked by rings).

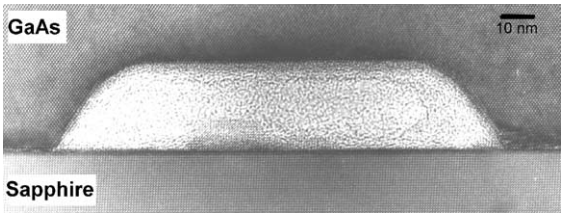

Fig. 5. Interface defect in $GaAs/Al_2O_3$ wafer bonding. The high-resolution TEM cross section shows the [1 1 1] and [1 0 0] oriented boundaries of the precipitate within the GaAs wafer. The precipitate is filled with Ga-rich and As-rich compounds.

be suppressed in GaAs/Si wafer bonding followed by an annealing procedure at elevated temperatures. Instead of using silicon wafers, 3 in silicon-on-sapphire (SOS) wafers with 500 nm of epitaxial silicon were bonded to GaAs. Due to the low thermal mismatch between GaAs and sapphire, the thermally induced mechanical stress is insignificant over a wide temperature range [6]. The bonding of SOS/GaAs was performed under arsenic pressure at 800°C for several hours. A high-resolution TEM cross section is presented in Fig. 4. Extra Si lattice planes are introduced at the GaAs/Si bonding interface to balance the lattice mismatch of 4.1%. Precipitates at the GaAs/Si interface, which contain mostly amorphous material, are occasionally observed with diameters ranging from 5 to 20 nm.

5. $GaAs/Al_2O_3$ bonding interfaces

Precipitates were also found at the bonding interfaces of GaAs and Al_2O_3 (see Fig. 5). The wafers were bonded as received after flushing in hydrogen atmosphere at a few hundred degrees centigrade. Further annealing at 500°C for several hours was necessary in hydrogen to maximize the bonding energies. Precipitates at GaAs/Al_2O_3 interfaces are settled in the GaAs. Since diffusion velocities in Al_2O_3 are rather low at the applied temperature, the defects contain mostly gallium-rich and arsenic-rich precipitates [10]. A closer look at the interface by plan-view TEM investigation reveals unbonded channel-like regions with strong bending contours. These channels can be responsible for the growth of precipitates by providing the mass transport to the interface.

6. Al_2O_3/Al_2O_3 bonding interfaces

Annealing temperatures near 1200°C are required to increase the interface energy of r-cut Al_2O_3/Al_2O_3 bonded wafer pairs to the binding energy of covalent bonds. At these high temperatures, a change of the interface morphology to form low energetic grain boundaries is evident. Wafers with small miscut show atomic steps or terraces at the surface. These steps are moveable during high temperature annealing. In bonded wafers with small surface miscut voids or negative crystals are achieved at the interface. The arrangement of well-ordered voids is shown in the plan-view TEM in Fig. 6. The density of the voids, which is in the range of $10^8\,cm^{-2}$, can be reduced by increasing the annealing time. The ripening of the voids continues at the gain of size.

Conclusively, bonding related defects and imperfections at the interface were observed in many integrated materials. At elevated temperatures, the diffusion length increases for impurities and interstitials within the considered material. Grain boundaries, interfaces or dislocations, however, reduce the diffusion length and

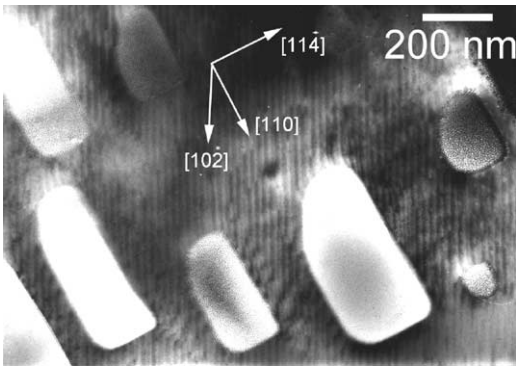

Fig. 6. Voids formation at the Al_2O_3/Al_2O_3 bonding interface revealed by plan-view TEM. During further annealing at 1200°C the density of voids is reduced while the diameters increase. The driving force for changing the surface morphology is to lower the surface energy of bonded wafers with rotational misorientation and surface miscut.

are attractive nucleation centers for the generation of voids, precipitates and novel crystalline phases. The bonding interface of two wafers is due to the material contrast, due to a miscut of the wafers and due to rotational misorientation between the two wafers. Avoiding high temperatures in dissimilar materials integration, e.g. by low-temperature bonding techniques, is required to prevent the defect formation at the bonding interfaces.

Acknowledgements

Dr. N.D. Zakharov and Dr. G. Kästner are kindly acknowledged for the TEM micrographs and discussions.

References

[1] Q.-Y. Tong, U. Gösele, Semiconductor Wafer Bonding, Wiley, New York, 1999.
[2] P. Kopperschmidt, et al., Appl. Phys. Lett. 70 (1997) 2972.
[3] C. Chen, et al., Philos. Mag. A 80 (2000) 881.
[4] E. Schroer, et al., Appl. Phys. Lett. 70 (1997) 327.
[5] G. Patriarche, et al., J. Appl. Phys. 82 (1997) 4892.
[6] P. Kopperschmidt, et al., Appl. Phys. A 64A (1997) 533.
[7] P. Kopperschmidt, et al., Appl. Phys. Lett. 74 (1999) 374.
[8] A. Borghesi, et al., J. Appl. Phys. 77 (1995) 4169.
[9] G. Patriarche, et al., Appl. Surf. Sci. 164 (2000) 15.
[10] P. Kopperschmidt, et al., Proceedings of the 23rd ICPS, World Scientific, Singapore, 1997, p. 967.