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Sodium outdiffusion from stacking faults as root cause for the recovery process of potential-induced degradation (PID)

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Abstract

Potential-induced degradation (PID) is currently one of the most important and prominent module degradation mechanisms leading to significant yield losses. It was shown that Na decorated stacking faults are responsible for this degradation mechanism of the solar modules. Additionally, PID can be recovered by an applied reversed voltage to the one causing PID. In this contribution both a thermal and an electrical recovery were performed. By in-situ thermal recovery and subsequent microscopic investigations the recovery process will be clarified. It is shown that Na causing PID diffuses out of the stacking fault during the thermal recovery process resulting in vanishing of the PID-s shunts. The stacking fault originally causing PID-s can still be verified by its atomic structure after recovery, now without any Na decoration. The clean stacking fault is not electrically active and thus is not influencing the electronic properties of the solar cells anymore. Finally, a qualitative process explaining the recovery is proposed.

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Keywords: Potential Induced Degradation; PID; Solar Cell; Recovery; Module Defect; Sodium; Diffusion

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1. Introduction

One of the most important advantages of the photovoltaic (PV) technology is their low cost of maintenance and long lifetime of over 30 years. Nevertheless, several degradation mechanisms can decrease solar efficiencies or destroy PV modules. Potential-induced degradation (PID) of crystalline Si solar cells is one of the main degradation mechanisms and has been intensively investigated since first publications reported the effect [1-3]. In conventional PV systems under working conditions, a voltage difference of a few hundred volts between the framing and the solar cells of a module can occur in dependence on the grounding of the solar system. If the modules/cells are not resistant to PID, the degradation mechanism can result in yield losses of 20 percent or more within a period of one year. According to recent publications, the PID shunting effect (PID-s), which decreases strongly the parallel resistance RP of the modules, is the most relevant type of PID [4,5]. However, it has also been shown that PID-s can influence the recombination behavior of the solar-cell [4,6].

In previous publications [7,8] we have shown that PID-s can be traced back to single sites independent on bulk crystal defects such as dislocations and grain boundaries. It has been shown that PID-s is caused by stacking faults decorated with a Na area density of about 1015 cm-2, which is equal to a planar atomic monolayer. This leads to shunting through a thin quasi metallic layer, hence an ohmic channel across the p-n junction. The shunting mechanism is discussed in [5]. Interestingly, various authors have reported a recovery of the PID-s effect by a reverse potential with respect to the one originally causing PID [2,9,10,11]. In this contribution thermal and electrical recovery processes are applied to PID degraded solar cells. The electrical properties of the solar cells are analyzed during recovery. The root cause for the thermal recovery process will be investigated in detail down to an atomic level. Finally, in a first model we will focus on explaining the thermal recovery process.

2. Experimental details

The solar cells investigated were PID prone screen printed multicrystalline silicon solar cells of the first generation. The PID degradation was conducted using the PID tester PIDcon by Freiberg instruments at +600 V and 80 °C [6]. The consecutive recovery was done either as an electrical recovery process by –600 V and 80 °C by means of the PIDcon tester or as an thermal recovery at a temperature of 250 °C. The thermal recovery was performed in an environmental electron microscope (ESEM) giving the opportunity to investigate the PID shunt sites by electron beam induced current (EBIC) with high spatial resolution during the recovery progress. Nanoscopic studies were performed by preparing silicon lamellas by focused-ion beam (FIB) technique. Electron dispersive x-ray (EDX) analyses and high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) were performed in a FEI TITAN TEM.

3. Experimental results

3.1 The recovery process

The recovery process was performed by two different methods: an electrical and a thermal recovery. In Figure 1(a) the parallel resistance RP in dependence on the test period of a solar cell under a foil and glass stack is shown. The degradation was performed in the PIDcon tester as described in [6]. The electrical recovery was achieved by a reverse voltage treatment of 600 V (opposite polarity with respect to the one causing PID) at 80 °C. A recovery and hence an increase of RP can be observed (see Fig 1(a)). However, within the test period the parallel resistance is not recovered completely. Nevertheless, the rise of RP is sufficient to recover the solar cell parameters under illumination such as the efficiency, short circuit current or fill factor as it was shown by Pingel et al. [12] as well.

In case of Fig. 1(b) the result of the thermal recovery process is shown. Thermal recovery was also already performed by various authors for PID recovery [13]. The thermal recovery was performed by a temperature of 250 °C only. Here, a dark I-V curve before and after thermal recovery of a piece of a solar cell is shown. The PID-s affected solar cell suffers clearly from ohmic shunting resulting in a linear characteristic around 0 V. After recovery this linear behavior has vanished and the I-V characteristic shows the typical diode behavior as it was observed before PID degradation. Therefore, PID-s can be recovered by voltage and temperature treatment. Generally, in both

cases the result was the same, hence the parallel resistance increases significantly and the solar parameters recovers nearly completely in both cases. In the following only in-situ thermal recovery is performed.

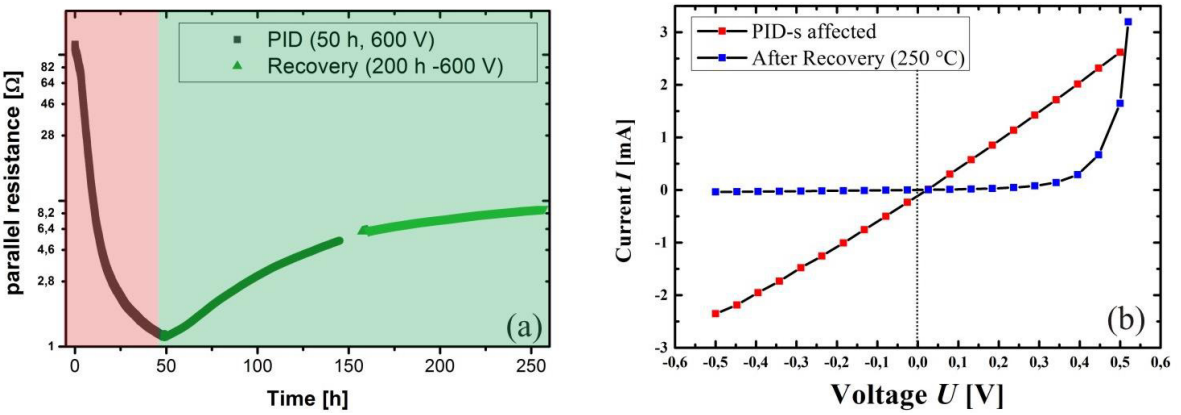

Fig. 1. (a) Parallel resistance in dependence on the degradation and electrical recovery time, respectively. The red colored region shall visualize the degradation process (+600 V) and the green region the recovery process (-600 V). (b) I-V Curves of a small piece of a solar cell after PID-s degradation (red curve) and after thermal recovery (blue curve)

3.2 Microscopic localization of a PID-s site before and after thermal recovery

In Figure 2(a) a PID-s site (marked with a dotted circle) of a PID-s affected solar cell can be seen by its decreased EBIC signal in an EBIC investigation at 20 kV acceleration voltage. The typical spot like occurrence is observed. Under low acceleration voltage (3 keV) (inset in Fig. 3(a)) and hence low penetration depth of the accelerated electrons, the PID-s site shows up as a line shaped defect caused by the Na decorated stacking fault which is penetrating the surface at this line (marked with a white line in the inset). After thermal recovery at 250 °C for 2,5 h both the shunting behavior of the solar cell (see Fig. 1(b)), as well as the PID-s site (Fig. 2 (b)) have vanished. Therefore, it can be assumed that the PID-s site is recovered. The white dashed line in Fig. 2(a) and (b) is marking a grain boundary and shall guide to the prominent region of the PID-s site. By in-situ EBIC measurements during thermal recovery it could be shown that the recovery process is not abrupt but rather gradually (not shown here). Not all PID-s positions vanish at the same time. Hence the recovery process seems to depend on a further influence perhaps such as the Na concentration within the stacking fault. The former PID-s position in Fig. 2 was chosen for further investigations on a nano-scale. The low energy EBIC measurements in the inset of Fig. 2(a) and the surface morphology give the possibility of a target preparation. The position of the TEM lamella is perpendicular to the white line and hence perpendicular to the puncture line of the stacking fault and the surface plane in the inset in Fig. 2(a). Exactly at this position a lamella with a final thickness of about 90 nm was prepared by focused ion beam (FIB) technique. Findings will be compared to previous results of PID-s sites. The investigated solar cell was of the same type, so a comparison is justified.

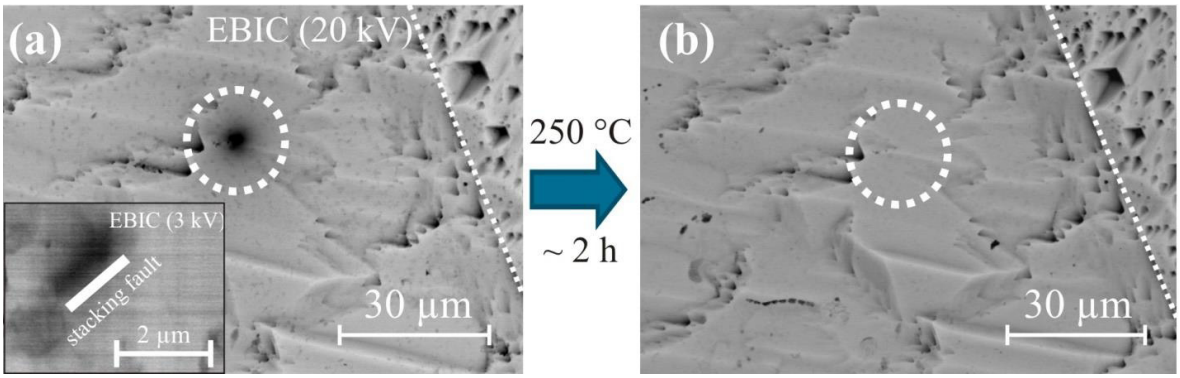

Fig. 2. EBIC measurement (20 kV) at a PID shunt site before (a) and after (b) a thermal recovery process. The dotted line is marking a grain boundary. The PID-s site has vanished after the recovery process. The inset in (a) shows the PID-s defect before recovery at low electron acceleration voltage (3 kV) and hence with an increased lateral resolution for further microscopic research. The puncture line of the stacking fault with the surface is marked by the white line.arately. Below is an example which the authors may find useful.

3.3 Microstructural EDX analyses of PID-s sites before and after thermal recovery

In Figure 3 STEM/EDX measurements of the lamellas before (Fig. 3(a)) and after (Fig. 3(b)) thermal recovery are shown. The EDX results of the PID-s affected lamella (without recovery) were already published in [7] and are cited for comparison. It was shown that the shunting type is caused by an aggregation of Na at the stacking fault plane. For a detailed discussion of the shunting process please see [5]. Interestingly, it was shown too that the Na concentration in the oxide layer in between SiN and Si is strongly increased. Furthermore, the concentration of Na within the stacking fault near the oxide layer is slightly decreased.

In Fig. 3(b) STEM/EDX measurements at the lamella of the former PID-s position after thermal recovery (Fig. 2) are shown. After a thermal recovery the stacking fault can be still located but a Na decoration of the stacking fault cannot be proven by EDX even with higher integration time compared to the measurement performed at the PID-s site in Fig. 3(a). Additionally, the lateral resolution was decreased to increase the measured EDX signal for a better visualization. Therefore, it can be concluded that during recovery the Na contamination has diffused out of the stacking fault. However, a small amount of Na seems to be still present in the oxide layer. This is visualized by an EDX line scan along the white arrow in Fig. 3(b). In Fig. 3(c) the EDX signal intensity of nitrogen, sodium and oxygen is shown as a function of the position (depth). A slightly increased Na signal within the oxide layer can be seen but by far lower compared to the results of the PID-s shunt. Note that the oxide layer and hence the Na signal in the recovered sample is broadened since the surface is tilted with respect to the lamella plane and not perfectly perpendicular to the beam plane. However, the stacking fault plane is perpendicular to the lamella plane and hence the Na signals are comparable.

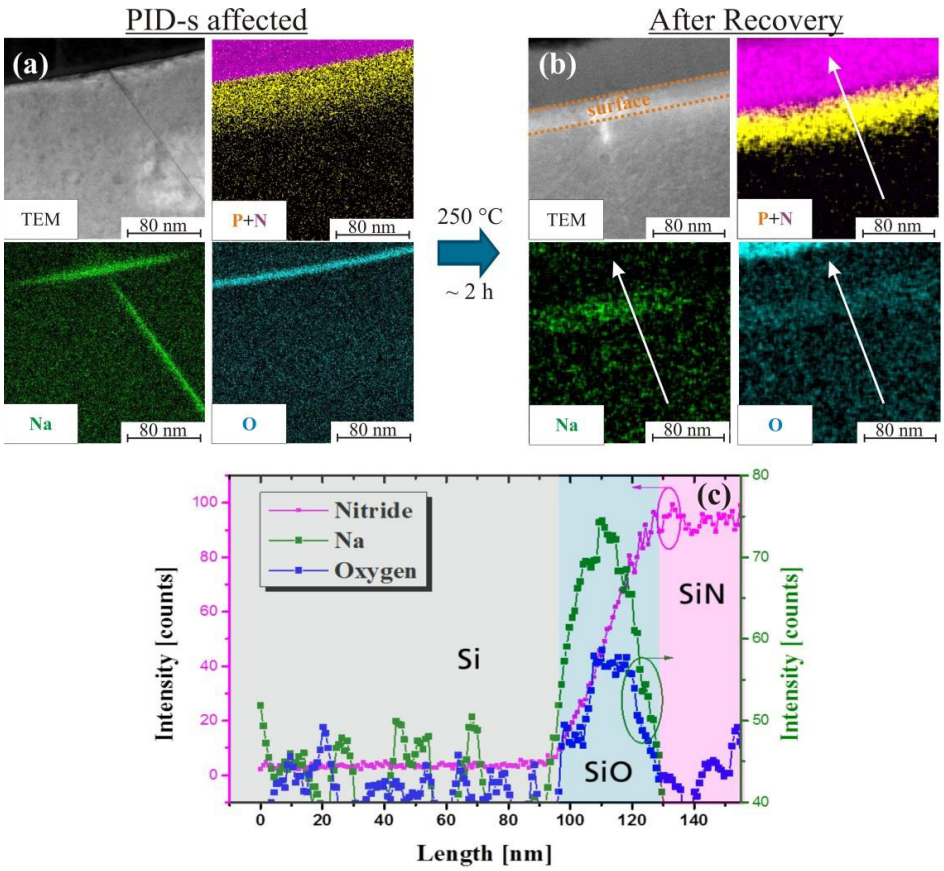

Fig. 3. EDX measurements of a TEM lamella before (a – taken from [7]) and after (b) thermal recovery of a PID-s affected solar cell. Along the white line in (b) an EDX line scan was performed and is shown in (c). Still a slightly increased Na signal can be measured within the oxide layer.

3.4 *STEM investigation of PID-s sites before and after thermal recovery*

In Fig. 4 HAADF STEM investigations before (a) and after (b) thermal recovery of PID-s causing stacking faults are shown. Theoretically, a stacking fault is just a failure in the symmetric order of the silicon structure and hence it should be possible to visualize the crystal structure clearly. However, before recovery (PID-s affected) the perfect silicon structure is strongly disturbed most likely by the Na atoms and/or the associated stress field leading to the dark region around the stacking fault (see marked region in Fig. 4(a)). After recovery (see Fig. 4(b)) the crystal structure and the disorder of the stacking fault can now be clearly visualized. Therefore, it is obvious that Na is not present at the stacking fault anymore. The “clean” stacking fault has no detrimental electronic influences near the SiN/Si interface and hence is not causing a shunting or an increased depletion region recombination as it can be seen in the EBIC measurement after recovery in Fig. 2(b). Such an undisturbed stacking fault was never observed in case of a PID-s causing stacking fault.

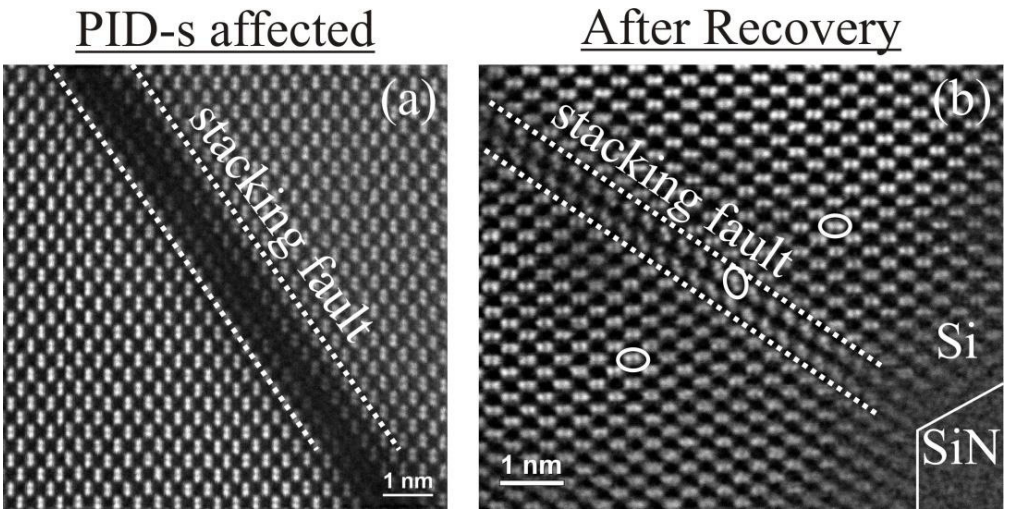

Fig. 4. HAADF STEM investigations before (a) and after (b) thermal recovery. The stacking fault is strongly disturbed before thermal recovery leading to the dark region around the stacking fault. After recovery the stacking fault is undisturbed, which may be explained by the out-diffusion of Na during thermal recovery.

4. The thermal recovery model

First, based on the obtained results it can be clearly concluded that Na decorating the stacking fault is reversibly inducing the shunting behavior of individual stacking faults. The in- and out-diffusion of Na at various is causing PID-s and thermal PID-s recovery on cell and module level. After recovery the PID-s sites cannot be detected by EBIC and the former PID-s sites show no influences on the electronic property of the solar cell anymore. At the position of the former PID-s shunt a stacking fault can still be observed by TEM. However, Na is not present at the stacking fault plane anymore as measured by EDX and which is finally confirmed by HAADF STEM measurements. In case of a Na decorated stacking fault its crystal structure is strongly disturbed and cannot be visualized by STEM. After recovery the Si matrix is undisturbed and the crystal structure of the stacking fault can be easily visualized. The crystal disorder of the stacking fault is now visible. Therefore, it can be concluded that Na decorating stacking faults is causing PID-s. During recovery Na diffuses out and is not present anymore at the stacking faults and the PID-s shunting is vanished, too.

The degradation process is explained in detail in [5]. Condensed, we assume that Na ions in the SiN antireflective coating are drifting towards the oxide layer due to the electric field. They accumulate at the SiN/Si interface and then diffuse (now as Na atoms) into stacking faults as visualized in Fig. 5. The formation (origin) of the stacking faults is not clear so far. Possibly the stacking faults are oxidation induced stacking faults during p-n junction formation or contact firing. If a specific Na concentration within the stacking fault crossing the p-n junction is reached, shunting will occur.

In the following only the thermal recovery will be discussed. We assume that during the thermal recovery process the Na atoms are diffusing out of the stacking fault into the oxide layer where the Na concentration is lower after the degradation has stopped. The slightly lower Na concentration near the oxide layer at the PID-s shunt in Fig. 3(a) could be a starting recovery process, i.e. a starting diffusion of Na back into the oxide layer. The increased temperature of 250 °C is accelerating the movement of the Na atoms and so accelerates the recovery process as well. In the oxide layer Na is relatively mobile [14,15] and will spread over the solar cell surface leading to a constant low Na concentration in the oxide layer near the stacking fault. In addition, Na can also diffuse back into the SiN layer (slower process) were it converts again to Na ions. If the Na concentration in the stacking fault is low enough, the electronic structure is undisturbed (as visualized in the band structure in Fig. 5 below) and the shunting and increased depletion region recombination will vanish. The degradation and recovery process is visualized schematically in the cross section in Fig. 5. The white arrows are marking the movement of Na (green dots).

The described process takes place without an applied voltage. In case of an electrical recovery an additional applied voltage across the SiN layer reversed to the one causing PID-s will help to ionize Na atoms and drift them away from the SiN/Si interface and so the recovery process will be accelerated since the Na concentration near the stacking fault will be additionally lowered. However, it is unclear so far what happens in different layers. The electrical recovery process will be in focus of an upcoming publication.

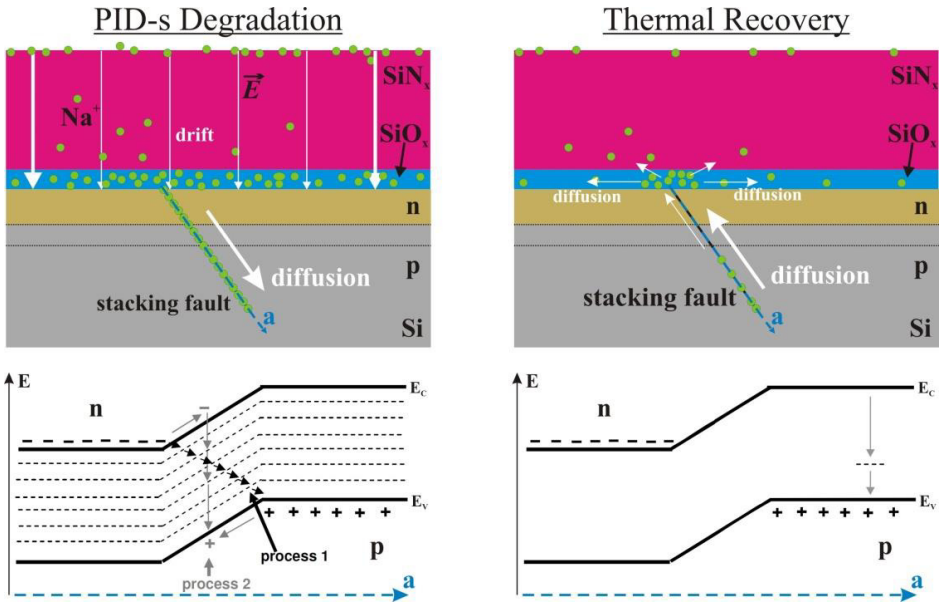

Fig. 5. Schematic model of the PID-s degradation and thermal recovery process. Shown is the cross section of a solar cell. The white arrows show the movement of the Na ions and atoms (green dots). The assumed band structure along the line "a" is visualized below. Without any sodium decoration the stacking fault has no influence on the electronic properties of the solar cell..

5. Summary

In this contribution thermal and electrical recovery of PID-s was shown through application of voltage and temperature at solar cell level. By in-situ thermal recovery in SEM it could be shown that the PID shunt gradually vanish during the recovery process. Microscopic studies revealed that the Na decoration of the stacking fault is not present anymore after thermal recovery. Hence the Na must be diffused out of the stacking fault during thermal recovery, leaving back a "clean" stacking fault, which is electrically not conductive and recombination active anymore. The Na removal is confirmed by STEM analyses on nanometer scale at PID-s stacking faults. The atomic structure of a PID-s affected stacking fault cannot be clearly identified due to the disturbed STEM contrast cause by Na decoration and accompanied stress fields. However, after thermal recovery the atomic structure of the stacking fault is clearly visible indicating the outdiffusion of the Na.

Within a final qualitative model it can be summarized that during the degradation process the Na diffuses into the stacking fault causing shunting. During recovery the Na diffuses out of the stacking fault therefore PID-s shunts vanish.

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