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Explanation of potential-induced degradation of the shunting type by Na decoration of stacking faults in Si solar cells



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ABSTRACT

Crystalline Si solar cells that exhibit potential-induced degradation of the shunting type (PID-s) are investigated on a microstructural level. Cell pieces with PID-shunts are imaged by SEM using the EBIC technique in order to investigate PID-s positions with high lateral resolution. ToF-SIMS depth profiles reveal Na accumulation localized at these shunt positions. Subsequently, cross-sectional FIB-lamellas of individual PID-shunts have been prepared. TEM is applied to a number of PID-s defects. TEM/EDX measurements reveal that stacking faults crossing the p–n junction are decorated with Na causing PID-s. These defects are further characterized by high resolution STEM methods down to the atomic scale. A model for the shunting mechanism in PID-s affected solar cells is developed. The results are discussed with respect to different shunting mechanisms.

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1. Introduction

Potential-induced degradation (PID) has been identified as a challenging reliability issue for solar modules manufactured from crystalline Si solar cells [1,2]. Especially PID of the shunting type (PID-s) can cause high power loss up to total failure of operating PV modules. PID-s has a high relevance, because it is frequently observed in existing PV installations [3]. The nomenclature "PID-s" is introduced in order to differentiate PID of the shunting type from other types of PID. (Different types of PID are corrosion of transparent conductive oxide layers in thin film modules [4] and the dissolution of antireflective coating (ARC) layers or the degradation of metallization in crystalline Si solar modules [2].) As stated in [1], PID-s is characterized by a reduction of the parallel resistance R_n . At proceeding PID-s this causes a drop of the fill factor, and thus the power output decreases. At high PID-s levels even the open circuit voltage V_{oc} and the short circuit current I_{sc} decrease due to massive internal short circuiting.

It was demonstrated that PID-s can be prevented by choosing alternative materials for solar module encapsulation, e.g. with quartz glass instead of soda-lime front glass or high electrical resistance thermoplastic encapsulants instead of ethylene-vinyl acetate [5]. The refractive index of SiN_x ARC is also reported to influence the PID-s susceptibility of solar cells [1,6]. It was shown that an increased refractive index is accompanied by resistance against PID-s. This is

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because the refractive index is associated with the Si proportion and therefore with the electronic conductivity of SiN_x layers. However, despite approaches for PID-s prevention are known and currently find their way into industrial application, it is necessary to improve the understanding of the PID-s mechanism. Na was identified to play a role for PID in general [2]. Analyses on cell level revealed an accumulation of Na at the interface between SiN_x and Si for PID-s affected cell regions [7]. Later it was discovered that both PID-shunts and Na accumulation at this interface are constrained to local spots (< 30 μ m) [8]. A spatial correlation between PID-shunts and Na accumulation was verified [8,9]. In addition, first hints towards an interplay between crystallographic stacking faults in the Si and PID-shunts have been reported [9]. In a recent work it was shown that stacking faults causing PID-s are decorated by Na. A model proposal for PID-s was briefly introduced in [10].

In this contribution the physical model towards a deeper understanding of PID-s based on advanced microstructural analyses will be discussed. For this purpose different monocrystalline Si solar cells have been investigated in order to achieve experimental data leading to a model for PID-s. Generally, for all investigated samples the results were the same.

2. Experimental

In order to be able to investigate PID-s shunts in more detail and without elaborate manufacturing of (mini-) modules, a PID test on cell level was developed. Basically, all PID-s prone cells

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show the same effects when they are stressed by means of the PID test on cell level. The advantage of the PID test on cell level is that after PID testing a clean cell surface without residues of encapsulants is obtained with low preparative effort. This is necessary for sophisticated microstructural analyses. The successful preparation of cells with permanent PID-shunts has been demonstrated at a number of more than ten mono- and multicrystalline Si-solar cells.

The PID test setup was developed to work on solar cell level (patent pending). It uses an electrode ($4 \times 4 \text{ cm}^2$) positioned above the cell surface separated from it by dielectric layers. According to conventional mini-module PID tests, comparable test parameters (80 °C, electrode at +600 V) have been chosen. This test procedure allows to obtain large cell fragments ($> 10 \text{ cm}^2$) or even complete cells without breakage.

PID-s affected monocrystalline cells with shallow alkaline front side texture have been prepared by means of this PID cell test. R_p of the cells was monitored during the PID test procedures. The validity of the PID test working on solar cell level has been proven by comparing results with degraded mini-modules and modules. PID-s affected solar cells investigated in this contribution have shown a strongly decreased R_p .

Before and after PID tests electroluminescence (EL) and dark lock-in thermography (DLIT) were used to obtain the locations of PID-related shunts. Pieces with PID-shunts have been further investigated by means of electron microscopy methods. Scanning electron microscopy (SEM) in a Hitachi SU70 equipped with an electron-beam-induced current (EBIC) system DISS 5 EBIC by point electronic has been used to find PID shunt positions. Characterization of PID-shunts has been carried out with acceleration voltages < 10 kV. Time-of-flight secondary ion mass spectrometry (ToF-SIMS) depth profiles have been acquired using a TOF.SIMS V apparatus (iontof) with a pulsed Bi⁺ primary beam. The sample surface has been gradually ion etched with an O_2^+ sputter beam. Cross sections at PID shunt positions have been prepared by means of focused ion beam (FIB) with Ga+ ions using a Zeiss FIB-SEM AURIGA CrossBeam. Cross sectional lamellas for transmission electron microscopy (TEM) have been cut out by FIB perpendicular to stacking faults and perpendicular to the (001) surface. TEM imaging of stacking faults has been performed in an FEI Tecnai G2 F20 microscope in order to verify the orientation of the stacking faults within the samples. The lamellas have been further thinned to a thickness of ~100 nm with Ar⁺ ions. High resolution TEM imaging and energy-dispersive X-ray spectroscopy (EDX) mappings with high sensitivity have been carried out using an FEI TITAN3 G2 60-300 apparatus equipped with an image spherical aberration (C_s) corrector and a Super-X EDX detector system. Structural properties of found defects have been further investigated employing a probe Cs-corrected FEI TITAN 80–300 electron microscope.

3. Results

3.1. SEM/EBIC and ToF-SIMS

After stressing mono- and multicrystalline Si solar cells in our PID testing setup for not laminated solar cells, the typical PID-s behavior could be observed. Within a testing time of 10-72 h R_p decreased in general down to some ohms. Subsequently, complete solar cells were taken out of the test setup and investigated by EL and DLIT in order to localize regions that exhibit a pronounced PID shunting. High resolution DLIT and SEM/EBIC investigations show that PID-shunts are always localized spots with a size of a few μ m [8,9]. The density of PID-shunts varies over some orders of magnitude from less than one per square centimeter to several hundred per square millimeter. It should be noted that in multicrystalline Si solar cells PID-shunts are not located at grain boundaries [10].

In the following, we will focus on microscopic investigations down to the atomic level. For this purpose, samples have been prepared from PID-shunted regions of monocrystalline solar cells for subsequent SEM/EBIC, ToF-SIMS and TEM analyses. Fig. 1 shows an EBIC image of a region with comparably high PID shunt density. Each dark spot represents one individual PID-shunt, due to the locally disturbed p-n junction [8,9]. The spots appear circular shaped with a diameter of $5-20 \,\mu m$ and with a pronounced halo. This extended spot size is due to the interaction radius for generation of electron-hole pairs is in the order of several microns. because the electron acceleration voltage is 30 kV. In contrast, an acceleration voltage below 10 kV results in an improved resolution of structural features of the shunts. Here, the shunts appear rather line shaped [9,10]. As verified in a number of SEM/EBIC investigations on mono- and multicrystalline Silicon solar cells, PID-shunts are assigned to stacking faults in {111} planes. Remarkably, PIDshunts are independent of other structural defects like grain boundaries or dislocations [9,10].

ToF-SIMS data acquired at the same sample region are shown in the framed overlay in the EBIC image in Fig. 1. The red dots within the frame represent the lateral distribution of Na at a depth corresponding to the interface between the SiN_x layer and Si substrate. The spatially resolved Na distribution has been extracted from a 3D depth profile of the Na⁺ signal acquired on an area of $500 \times 500 \,\mu$ m. Obviously Na accumulates at positions which coincide with PID-shunts observed in EBIC imaging. The inset graph in Fig. 1 shows the depth distribution of Na measured at shunt positions. A significant increase of the Na signal (red line) is clearly visible at the SiN_x/Si interface. The interface (see arrow) is indicated by the declining Si₂N⁺ intensity (blue line).

3.2. TEM and High resolution EDX analysis

In order to investigate structural properties and elemental composition of individual PID-shunts on a nanometer scale, TEM



Fig. 1. EBIC image of a monocrystalline cell region with a high density of PIDshunts acquired at an acceleration voltage of 30 kV. The overlay in the EBIC image shows the distribution of Na at the SiN_x/Si interface measured by ToF-SIMS. The graph (inset) shows the depth distribution of Na at shunt sites in comparison with the Si₂N signal being an indicator for the SiN_x/Si interface. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

experiments including elemental analyses (EDX) have been performed. Using a target preparation technique based on SEM/EBIC and FIB, several PID shunts have been localized, prepared and analyzed in greater detail. Cross sections at nine investigated PID shunts revealed stacking faults in {111} planes. Thus, previously published results by SEM/EBIC and TEM could be verified on broader statistical basis [9].

Fig. 2 shows an example of a PID-s stacking fault with its plane oriented perpendicular to the TEM lamella surface and inclined to the surface of the solar cell. The TEM brightfield image in Fig. 2 on the left side gives an overview of the stacking fault. The Pt protection layer, which is needed for the FIB preparation, appears black. Below the Pt layer the \sim 70 nm thick SiN_y layer appears dark grey. Crystalline Si appears light gray in this TEM image. A stacking fault in the Si crystal, reaching from the surface to a depth of nearly 2 µm, is visible as a thin dark line. Elemental composition information is obtained by EDX in scanning TEM (STEM) mode. The corresponding EDX maps on the right hand side show the elemental distribution of Na, O and N near the Si interface. The SiN_x layer is indicated by a high EDX signal for N. An interlayer that contains O is clearly detected in the SiN_x/Si interface region. It is assigned to a thin SiO_x interlayer. From Na-EDX maps it can be derived that Na is located along the stacking fault. Na is observed throughout the stacking fault (not shown here) down to its lower part (inset in TEM image). In addition Na is also detectable in the SiO_x interlayer where the stacking fault touches the interface. Moreover, the Na EDX signal is weakened in the uppermost 50-100 nm of the stacking fault.

A quantitative evaluation of the EDX data for Si and Na yields an estimation for the areal density of 6×10^{14} and 3×10^{14} Na atoms per cm² in the stacking fault plane for depths of (80 ± 40) nm and (1.6 + 0.1) µm, respectively. In comparison, ToF-SIMS also revealed a signal equivalent to an areal density of $\sim 10^{15}$ Na/cm² [10]. Therefore, we assume a density of Na within the stacking fault in an order of magnitude that corresponds to one Si monolayer. It should be noted that a similar Na distribution along the stacking faults has been verified for two other TEM investigations of PID-s affected stacking faults. Other foreign metals than Na have not been detected. In some cases also small amounts of O were found along stacking faults.



Fig. 2. On the left is a brightfield TEM image of a stacking fault affected by PID. The small images on the right represent EDX mappings acquired in STEM mode at this stacking fault near the interface between Si and SiN_y. A Na-EDX map of the lower part of the stacking fault is shown in the inset on the left.

3.3. TEM and atomic structure analysis

The atomic structure of PID-s stacking faults has been further studied by STEM. An overview of such a PID-s planar defect in cross section ([110] orientation) is shown in the low-angle annular dark-field (LAADF) image in Fig. 3. The LAADF technique is especially useful to image defects by their strain fields. Local atom displacements cause de-channeling of the imaging electrons [11]. The strained regions thus appear bright in comparison to the unstrained regions. In Fig. 3 the stacking fault (which is filled with Na, like the defect shown in Fig. 2) thus appears as a thin, heterogeneously bright line and penetrates the Si from the surface (i.e. the interface between SiN_{r} layer and Si) down to a depth of about 3.4 µm.

The orientation of the defect line with respect to the (001)oriented surface proves that the defect is in a {111} plane. Highresolution annular dark-field STEM is employed to characterize the atomic structure of the planar defect. In the following the crystallographic details are further addressed.

The high-angle annular dark-field (HAADF) image in Fig. 4 illustrates the atomic structure of a typical $9 \text{ nm} \times 9 \text{ nm}$ cutout from the defect. In the diagonal of the image a dark stripe is distinctly noticeable lying parallel to the $(\overline{1}11)$ atomic planes of the Si crystal, which indicates a stacking fault. However, a clean intrinsic stacking fault should be characterized by a single layer of rotated dumbbells and in an extrinsic stacking fault there should be two rotated dumbbell layers [12]. In contrast to a clean stacking fault, the atom dumbbells, being directly adjacent to the dark stripe in Fig. 4, appear darker than the Si dumbbells in the bulk. Furthermore, they have the same orientation as the bulk dumbbells which is parallel to $[00\overline{1}]$ in the projection onto the paper plane. This phenomenon demonstrates a structural modification of the original stacking fault by the potential-induced degradation process, which yields the Na agglomeration at the fault plane as already described (cf. Fig. 2) and also proven by EDX at the defect under discussion. The arrangement of Na atoms within the fault thus appears to induce moving of Si-atoms in the neighborhood, which finally reorients the Si dumbbells in the projection. However, directly next to the dark stripe there are also dumbbells with an orientation as in the original stacking fault, which will be shown in Fig. 6.

The dimensions of the defect as well as its HAADF contrast are considered in detail in Fig. 5, which shows an unprocessed cutout of Fig. 4. The image has been rotated to align the $(\overline{1}11)$ atomic planes



Fig. 3. Low-angle annular dark-field (LAADF) STEM image of a planar defect, which penetrates the Si starting from the interface between Si and SiN_x down to a depth of about 3.4 µm.



Fig. 4. HAADF image showing the atomic structure of a PID-s fault.



Fig. 5. Dimensions of a PID-s affected stacking fault determined by a brightness profile (top). The corresponding HAADF image with the defect in the middle (bottom) is an unprocessed cutout of the HAADF image in Fig. 4.

to the vertical image edges. Above the image the corresponding brightness profile is shown. The brightness is averaged over the height of the cutout and is plotted against the cutout width.

Slightly off the defect the $(\overline{1}11)$ -planes are arranged in their typical bulk distance of 0.314 nm. They exhibit a nearly constant high brightness. In the close surrounding of the stacking fault (about 1.5 nm to each side) the brightness maxima of the $(\overline{1}11)$ -planes decrease. The defect stripe itself stands out by the lowest brightness in the image. However, the stripe does not show a continuous contrast but rather a local brightness maximum (see the middle of the profile). As the HAADF contrast is proportional to the mean atomic number in the investigated volume to the power of about 2 [13], the local brightness minimum allows an estimation of the mean atomic number in the middle of the defect to about 6-7. This indicates the incorporation of additional atoms with an atomic number smaller than 14 (the atomic number of Si) as well as of vacancies. In addition, local atomic displacements have to be considered, which also yield a decrease in brightness by de-channeling. That phenomenon is assumed to mainly cause the decrease in the brightness of the Si-dumbbell columns in the surrounding of the defect stripe, because a bright contrast was observed there in the LAADF image (cf. Fig. 3).

The distance of the adjacent Si dumbbells on both sides of the investigated fault is 0.57 nm. This distance is distinctly smaller than

that of the Si dumbbells adjacent to an extrinsic stacking fault, which is characterized by a double fault layer. The observed distance is rather in the range of an intrinsic stacking fault (being characterized by a single fault layer) [12]. Thus, assuming an intrinsic stacking fault, the measured stripe width of 0.57 nm corresponds to a widening of the original stacking fault by about 0.25 nm. This supports the thesis that Na atoms aggregate in the original fault plane. The fact that the Na atoms have not been imaged as bright spots by HAADF might be attributed to an irregular incorporation of Na, i.e. the positions of Na atoms might differ along the thickness of the lamella. Moreover, a lower density of atoms compared to the bulk Si has to be taken into account. The incorporation of Na in the fault plane appears to locally induce a re-arrangement of Si atoms at the fault as shown in Fig. 6a and b. It may be speculated that at the fault the Na atoms form locally arrangements comparable to that in the Zintl phase NaSi. In the lower part of Fig. 6b Si dumbbells can be seen adjacent to the stacking fault maintaining the original fault orientation. In contrast, dumbbells in the same plane turn towards the bulk orientation in the upper part of Fig. 6b. That might have been induced by an arrangement of Na above the dumbbells forming triangle units as marked in Fig. 6b. In Fig. 6a all Si dumbbells are realigned in the bulk orientation which is consistent with an annihilation of the fault.

4. Discussion

All investigated samples showed typical degradation of R_p in a comparable time scale and under comparable conditions with respect to mini-module based PID-tests [7–9]. It is commonly accepted that in (mini-)module PID-tests the degradation process is the same as it is observed in field installations, but under accelerated conditions. Therefore we strongly believe that the observed PID-shunting of our samples is similar to what is seen in fielded modules.

The presented results clearly indicate the major role that stacking faults play for PID-s. In particular, it is obvious that stacking faults with a length of several micrometers extend from the SiN_x/Si interface through the p–n junction into the p-doped Si base material. It was proven by several measurements that the stacking faults are decorated with Na. It is assumed that the Na contamination of the stacking faults takes place during PID stressing of the solar cell, leading to a modification of the electronic structure of the stacking fault towards an ohmic channel between the n⁺ layer and the p-doped base of the solar cell. As a result a local PID shunting is induced.

However, several issues related to the formation of the stacking faults, the Na contamination and the resulting properties of the atomic and electronic structure have to be discussed. In this context, we would like to indicate possible steps for further experimental and theoretical approaches to a microstructural understanding of the mechanisms of PID-s. Finally, we would like to address the question how to distinguish PID-s from other forms of PID.

4.1. Structural properties and formation of stacking faults

The width of an intrinsic stacking fault is about 0.32 nm, whereas a stacking fault of the extrinsic type measures about 0.63 nm [14,15]. Although Na is incorporated into the PID-s defect, its width of 0.57 nm is smaller than that of an extrinsic stacking fault. Thus, the original defect is supposed to be an intrinsic stacking fault before the degradation. In addition to the widening of the original stacking faults, the defects seem to be structurally modified as a consequence of the PID process. The arrangement of Na atoms within the fault seems to induce a shift of Si-atoms in the neighborhood, which finally reorients the Si dumbbells in the projection.



Fig. 6. Re-arrangement of Si atoms in the dumbbells being located adjacent to the fault. In (a) all Si dumbbells are realigned in the bulk orientation. In (b) the dumbbell rotation of the original stacking fault is locally maintained (marked by the lower red oval). Above, Si atoms also seem to shift by arrangement of Na nearby (yellow), thus forming triangle units. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

However, at the present state of research, all planar defects enabling Na to diffuse into the Si have to be taken into account. In that context especially oxidation-induced stacking faults have to be considered, which are known to grow from interfaces between Si and SiO_x during oxidation or annealing [16]. That brings particularly the POCl₃-diffusion step of the solar cell process into the focus of the discussion [17]. But in contrast to the intrinsic stacking faults, which are assumed in this work, stacking faults being induced by oxidation are commonly assigned to the extrinsic fault-type [18]. Note that oxide precipitates were also found near to PID-s affected stacking faults by EDX (not shown here).

Investigations of heat-treated (and thus 'regenerated') PID-s defects as well as of stacking faults at cells (that are not affected by PID) are planned. Furthermore, density functional theory (DFT) calculations will be performed to verify the structure changes by implementing Na in the defect. That should allow to calculate the density and energy of electronic states due to incorporation of Na into Si-stacking faults explaining the shunting mechanism.

Since PID-affected multicrystalline cells also exhibit PID-shunts with equivalent linear shape [10], it is expected that the root cause for PID-s is the same for both mono- and multicrystalline cells. Further structural defects, i.e. dislocations and grain boundaries, seem to play a minor role with respect to PID-s.

4.2. Transport of Na into the stacking faults

The simple assumption of a homogeneous electric displacement field like in a parallel plate capacitor would result in an electric potential difference of less than 0.05 V over the SiN_x layer, when 1 kV is applied over 3 mm glass, 300 µm encapsulant and 80 nm SiN_x layer. In [19] it is stated that a potential of at least a few volts across the SiN_x layer is necessary to cause PID-s. In addition to the observation of leakage currents [5] (caused by mobile ions in an electric field) this leads to the consideration of charge pile up at interfaces when the mobility of drifting ions decreases from one material to the following. Exactly this pile up of charges (ions) is assumed to increase the potential across the adjacent dielectric. This implies that not only Na may be responsible for building up a high field across the SiN_x layer. In corona charge experiments [20] charges are applied directly to the SiN_x surface. However, for PID it is required that the electronic conductivity of the SiN_x layer is low [19], otherwise surface charges on the SiN_x layer would become neutralized. SiN_x ARCs are known to exhibit increased electronic conductivity at increasing refractive indices. It has been reported that layers with $n \ge 2.2$ cause resistance against PID-s [21].



Fig. 7. Schematic drawing of a solar cell cross section. An electric field across the SiN_x layer causes drift of Na^+ ions towards the Si interface. Na scatters in a thin interfacial SiO_x layer. Diffusion into stacking faults takes place. The lower drawing shows the proposed band structure along a decorated stacking fault. The current flow across a PID-s defect is shown at high level concentration (process 1, black) and at relatively low local level concentration (process 2, gray).

According to our findings that Na is found at stacking faults in cell regions, which have been exposed to PID stress, it is assumed that Na ions drift through the SiN_x layer under the influence of a strong electric field. This is visualized in the upper part of Fig. 7. Na may come from the surface, since contamination with Na is commonly observed on surfaces. Alternatively Na may also be resident within the SiN_x layer as a contaminant. Note that even small volume fractions of Na can lead to high areal concentrations when it is piled up in planes. As shown in Fig. 7, the Na ions are driven towards the SiN_x/Si interface and accumulate in the SiO_x interlayer. Their positive ion charge prevents further Na from drifting to the interface where Na piles up at the Si interface. Pure thermal diffusion of Na in SiN_x is low, while its diffusivity is much higher for SiO₂-like phases [22]. Therefore, Na may easily diffuse laterally inside the thin SiO_x interlayer (see also Fig. 2).

Stacking faults provide two-dimensional diffusion channels. In contrast, thermal diffusion of Na in Si bulk is low at room temperature [23]. Na is supposed to enter stacking faults from the SiO_x interlayer and then becomes neutralized by free electrons in the emitter. This neutralization allows further Na to follow through the SiN_x layer towards the Si interface. A decoration of the stacking fault by Na is supposed to create a shunt across the p–n junction (see 'Shunting mechanism').

In this model PID-s recovery could be explained as a diffusion driven process. When the outer field across the SiN_x layer is switched off, Na is able to slowly spread back from the stacking fault into the SiO_x interlayer and from that into the SiN_x layer by diffusion and electrostatic repulsion. Broad thermal back-diffusion into the SiN_x layer is delayed due to the low mobility of Na [22], leading to a slow regeneration [24]. Therefore PID-s recovery can be accelerated by means of reverse potential across the SiN_x layer. Dependent on the transport of Na ions back into the SiN_x layer, there is a concentration gradient enabling Na to diffuse out of stacking faults. The Na accumulations measured by ToF-SIMS in the SiN_x/Si interface region (see Fig. 1) are supposed to be the result of beginning out-diffusion of Na.

4.3. The shunting mechanism of Na-decorated stacking faults

The results presented here are not compatible with the electrostatic PID defect model proposed in [7], which assumed that the Na is lying within the SiN_x layer. Our previous TEM investigations (see also Fig. 3) might indicate that the Na atoms are microscopically distributed in the stacking fault not as a completely flat layer but rather quite inhomogeneous. One possibility would be to assume that the Na atoms convert the stacking fault into a thin guasimetallic layer, which could explain the ohmic conductivity across the p-n junction. Then the defect would act like the model for type-2 breakdown mechanism proposed in [25]. However, one may also assume that, within the p-type bulk material, the defect acts as a Schottky diode instead of an ohmic contact. On the other hand, a well-rectifying Schottky diode is only expected for an ideal metalsemiconductor contact. This Na-Si contact, however, can be expected to be highly disturbed and may be contains a Cottrell atmosphere of point defect levels around, which may convert it to an ohmic contact to the bulk, as it is observed here.

A second possible explanation has already been discussed in [10]. Implanted Na atoms as impurities on interstitial positions create donor states within the band gap in Si crystal bulk material [23,26]. In our case Na atoms are supposed to be constrained to the stacking fault plane, which yields a widening of the original intrinsic fault by about 0.25 nm. Metallic Na is characterized by a continuum of electronic states around the Fermi level. Therefore it is assumed that the Na atoms being concentrated at the fault plane lead to a band of gap states at multiple energies within the Si band gap, as sketched in Fig. 7. This figure shows the assumed band structure within a PID-s defect across the p-n junction. Here, it depends on the local defect level concentration how this defect acts electronically. (This may be related to the formation of a two-dimensional Mott-Hubbard system. as reported for Na adsorption on the Si (111) surface [27].) If the local defect level concentration in the PID-s defect is high, the defect orbitals of neighbored levels overlap, enabling hopping conduction. This is shown as "process 1" (black) in Fig. 7. This process does not need any thermal activation and therefore leads to an ohmic conductivity across the p-n junction.

At relatively low level concentrations we may already see interlevel recombination via levels of different energies located at the same place in the middle of the depletion region ("process 2", gray in Fig. 7). Here, the lateral overlap of neighboring defect orbitals is still too low to enable significant lateral hopping conduction. Then this defect leads to depletion region (2nd diode) recombination with a large ideality factor, as it has been described theoretically in [28] and has been found experimentally on PID-affected cells in [24]. Since this process needs thermal activation, it leads to a non-linear *I*–*V* characteristic.

4.4. Differentiation of PID-s versus other PID types

All present results have been obtained at samples which exhibit PID of the shunting type (PID-s). According to reports [3], this type is expected to represent the most occurring and most relevant type of PID. Therefore, it should be treated as a separate phenomenon. This implies a clear differentiation from other potential-induced module defects. Other PID phenomena are corrosion of cell connectors, dissolution of ARCs [2] and the 'polarization effect' proposed to base on a field effect resulting in increased recombination [29]. But in the latter reference *I-V* curves also clearly show a decreased R_p after PID. A dominating reduction of V_{oc} is not shown there, as it would be expected from increased recombination only. Therefore, it is not clearly deducible whether different phenomena had been observed in that work.

5. Summary

In this work PID of the shunting type (PID-s) has been investigated beginning with solar cells on the macroscopic level and down to the sub-nanometer scale. A decrease of R_p (shunting) is the dominating degradation effect for investigated p-type solar cells prone to PID. SEM/EBIC in top view revealed local PID-shunts. They are shown to be associated with Na accumulations found by means of ToF-SIMS at the interface between the SiN_x layer and Si. Obviously, a high potential above the solar cell promotes the drift of Na to the interface under the influence of an electric field across the SiN_x layer.

A number of individual PID-shunts have been investigated by TEM. All PID-shunts investigated with STEM/EDX exhibit aggregations of Na at planar crystallographic defects. According to detailed TEM investigations the defects are confirmed to be stacking faults. Considerations of stacking fault dimensions and the orientation of 'Si dumbbells' lead to the assumption that the stacking faults are of the intrinsic type. Thus, Na that penetrated the stacking fault plane seems to modify the arrangement of adjacent Si atoms.

These findings are interpreted in a way that Na occupies places in the stacking fault plane with a high density. Thus, a band of states is created filling the whole original band gap. This provides a high conductivity between n-doped emitter and p-doped base. The formation of such PID-shunts with a high density leads to PID-s.

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