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The role of stacking faults for the formation of shunts during potential-induced degradation of crystalline Si solar cells

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Mono- and multicrystalline solar cells have been stressed by potential-induced degradation (PID). Cell pieces with PID-shunts are imaged by SEM using the EBIC technique in plan view as well as after FIB cross-section preparation. A linear shaped signature is found in plan-view EBIC images at every potential-induced shunt position on both mono- and multicrystalline solar cells. Cross-sectional SEM and TEM images reveal stacking faults in a {111} plane. Combined TEM/EDX measurements show that the stacking faults are strongly decorated with sodium. Thus, the electric conductivity of stacking faults is assumed to arise under the influence of sodium ion movement through a high electric field across the SiN_x anti-reflective layer, resulting in PID.

In its most prominent form potential-induced degradation (PID) acts as a drastic reduction of the parallel resistance of silicon wafer-based solar modules. It has been shown that this is caused by shunting of solar cells in PID-affected regions of modules [1]. Sodium (Na) was suspected to play a crucial role for the PID effect [2]. Recent microstructural investigations at SiN_x antireflective coatings (ARCs) of PID-affected sites revealed Na to accumulate at the interface between the SiN_x and the Si material [3, 4]. Furthermore, time-of-flight secondary ion mass spectroscopy (ToF-SIMS) measurements yielded that Na is not uniformly distributed at the SiN_x/Si interface, but rather shows small spots (diameter <10 µm) with significantly elevated Na signal. These spots correlate exactly with PID-related shunts found by scanning electron microscopy (SEM) in electron beam induced current (EBIC) mode [4]. Recently it was discovered at monocrystalline Si solar cells that PID shunts are also correlated with crystallographic defects in Si. According to findings at cross sections the defects could be attributed to stacking faults [5]. It was already supposed that they play a major role in the formation of PID shunts.

This Letter aims for a generalization of this finding (towards multicrystalline Si solar cells) and for the detailed shunting mechanism at stacking faults. For this purpose mono- and multicrystalline p-type solar cells have been exposed to PID employing an in-house developed setup (patent pending). It uses an electrode positioned above the cell surface separated from it by dielectric layers allowing PID testing of cells without the need for mini-module manufacturing. Cells used for this work have been stressed with +600 V at 80 °C for different durations until PID led to significant shunting (reduced parallel resistance R_p), while R_p has been monitored in real time. Subsequent to PID stressing the cell surface was accessible without any breakage of the cell. In the following standard procedure the cells have been imaged with electroluminescence in order to localize regions with increased PID shunt density.

Square-centimeter sized cell pieces have been cut out for subsequent SEM investigations.

In direct comparison of EBIC images multicrystalline cells exhibit the same shunt signature as monocrystalline samples [5]. Round dark spots (low EBIC signal) with significant dark halos are visible at an electron acceleration voltage of 30 kV. In detail they appear as linear defects with a length of 10 µm or less at acceleration voltages below 10 kV. PID shunts have not been found at grain boundaries. Instead, PID shunts occur scattered inside individual grains. In Fig. 1a PID shunts are shown with EBIC (30 kV) on a grain of a multicrystalline cell with alkaline surface texture. The etch morphology ({111} planes) can be seen in EBIC due to a shadowing effect. The strong PID shunt marked with an arrow in Fig. 1a is shown magnified in the EBIC image (9 kV) in Fig. 1b. The visible dark line is clearly assigned to a stacking fault in a {111} plane crossing the surface, as it is deduced from its orientation with respect to visible {111} planes. Like at this example, the orientation of other shunt lines has been proven for mono- and multicrystalline Si solar cells at a number of >20 individual PID shunts in total including seven cross sections. All of them reveal such planes with {111} orientation hitting the surface and crossing the p–n junction.

Oxidation-induced stacking faults have been described by Ravi and Varker [6]. Their investigations have shown that these stacking faults may be electrically active under reverse bias if they cross the p–n junction of a diode perpendicular to the wafer surface [7]. According to generation–recombination centers in the close surrounding of the stacking faults they postulated that they may be decorated with impurities. The EBIC images in [7] show the same behavior as our PID-related defects. However, in contrast to the observed ohmic PID-shunts [5] they have been measured to exhibit a pronounced non-linear reverse *I–V* characteristic with some orders of magnitude lower currents in the considered reverse voltage range up to 5 V.

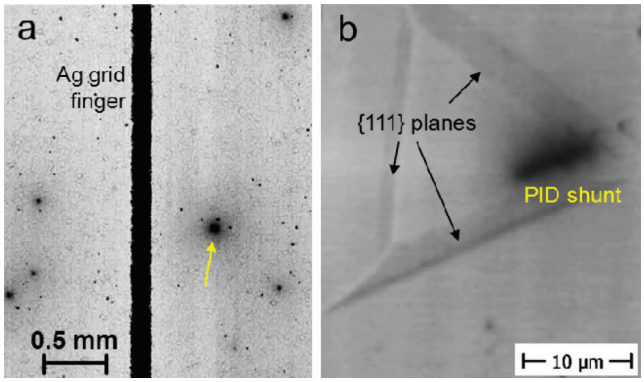

Figure 1 EBIC image (30 kV) with several PID shunts on a multicrystalline silicon solar cell (a). The yellow arrow points at the PID shunt, which is shown under higher magnification (9 kV) in the EBIC image in (b).

Presumably, the degree of contamination there was much below that in our case.

For the purpose of an elaborate ToF-SIMS experiment, first the SiN_x layer of a monocrystalline cell with PID-shunts was removed by O_2^+ ion etching on an area of 700 □ 700 µm^2 until the Si substrate was eroded to a depth of ~0.05 µm. In the following, a ToF-SIMS depth profile with increased sensitivity for Na was found inside the Si in PID-shunt regions, i.e. at the stacking faults. Figure 2 shows details of secondary-electron (SE) (a) and EBIC (b) images acquired at 30 kV. The corresponding ToF-SIMS ion images (Fig. 2c and d) are integrated over a depth profile between 0.05 µm and ~1 µm below the SiN_x/Si interface. The ToF-SIMS total ion image (Fig. 2c) proves congruence with the SEM/EBIC images.

A thorough estimation based on this ToF-SIMS depth profile measurement yields a number of ~10^8 Na-atoms per stacking fault up to the depth of ~1 µm. Projected on the stacking fault plane this corresponds to a density of ~10^{15} Na-atoms per cm^2. This number is in the same order of magnitude as the area density of Si atoms within a {111} plane. Thus, roughly a monolayer of Na can be assumed to lay in the stacking faults analyzed in Fig. 2.

Another hint for Na distribution alongside a PID-shunt related stacking fault has been found by means of SEM with energy dispersive X-ray spectroscopy (EDX) mapping at a cross section (not shown here). In order to prove this and for the purpose of better resolution a transmission electron microscopy (TEM) lamella was cut out of a PID-affected monocrystalline cell perpendicular to a stacking

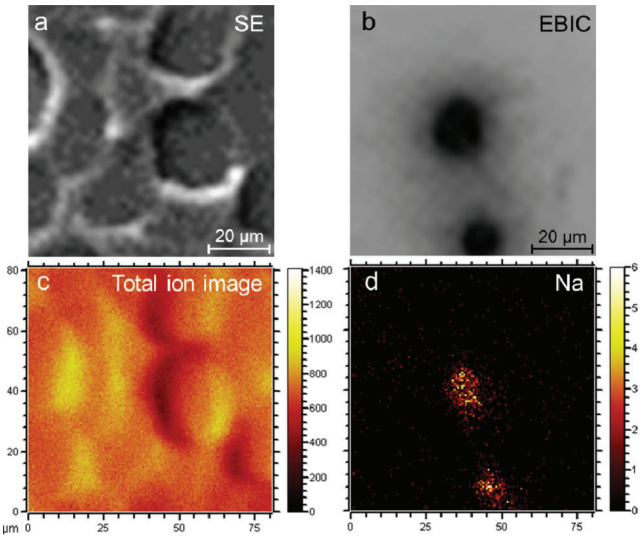

Figure 2 Small-section view (80 □ 80 µm^2) of a monocrystalline cell imaged by SEM (a, b). The ToF-SIMS images (c, d) have been integrated over a depth of 0.05 to ~1 µm below the SiN_x/Si interface after removal of the SiN_x layer. (a) Surface topography (SE image) in correlation to the total ion mapping (c). The corresponding EBIC view (b) shows dark spots at exactly the same two positions where Na is measured within the uppermost ~1 µm of Si substrate (d).

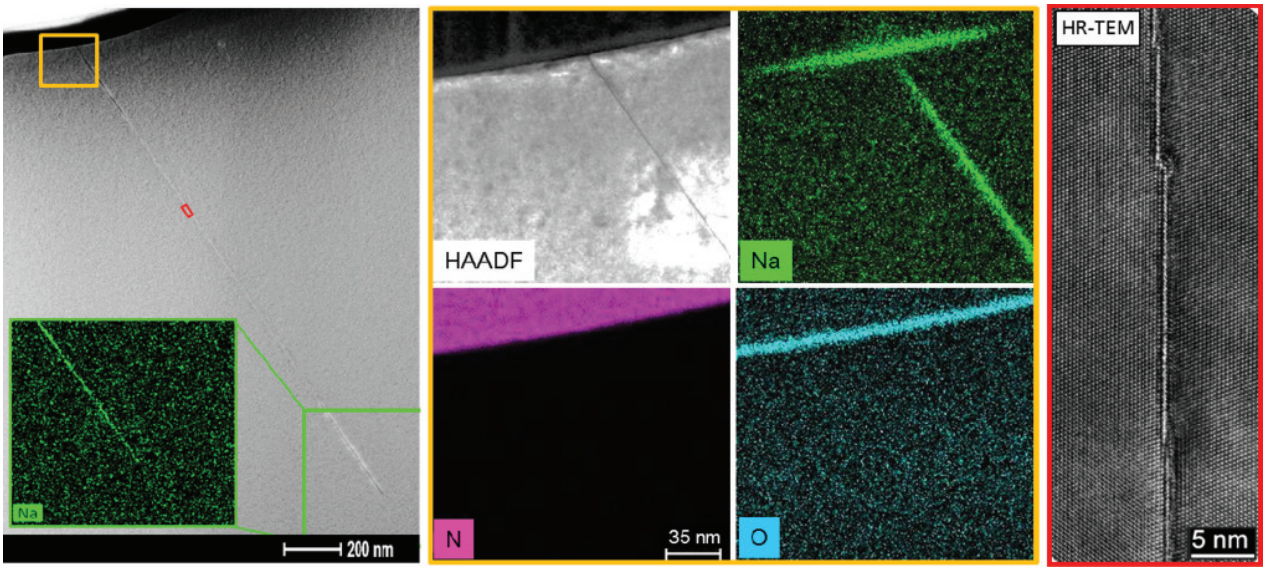

Figure 3 Transmission electron microscope characterization of a PID shunt in cross section: On the left a HAADF (high angle annular dark field) scanning TEM image shows an overview of a 2 µm-long stacking fault. Some structural details of the fault in the region of the red-marked cutout are illustrated by the C_s corrected high-resolution TEM image on the right. Note the steps in the fault plane. The included EDX intensity maps on the left and in the middle clearly demonstrate the agglomeration of Na at the fault and at the interface to the SiN_x layer. In addition, O, which was detected at the interface between Si and SiN_x, indicates a thin SiO_x layer.

fault and perpendicular to the {100} surface. This lamella was thinned to a thickness of ~100 nm. EDX mappings with high sensitivity have been carried out at this sample using a TITAN^3 G2 60-300 apparatus equipped with an image spherical aberration (C_s) corrector and a Super-X EDX detector system. Figure 3 shows on the left-hand side a dark field scanning TEM overview of the whole stacking fault that penetrates the Si up to a depth of 2 µm. EDX maps (Fig. 3, center) verify that Na decorates the stacking fault.

Most probably Na entered and diffused alongside the stacking fault in the course of PID. Furthermore, the Na concentration is also enhanced inside a very thin SiO_x (O signal) interlayer between Si and SiN_x directly above the stacking fault. It can be assumed that there Na has diffused out from the stacking fault after the PID process and due to preparation of the TEM lamella. Na is also found at high depths up to the end of the stacking fault ~2 µm below the surface (left inset in Fig. 3).

Note that the p–n junction is located at a depth of ~300 nm and therefore is within the zone influenced by the Na-decorated stacking fault. The image on the right-hand side of Fig. 3 shows a high-resolution TEM image in the middle of this stacking fault. In this image the stacking fault in a {111} plane is indicated by a bright line and a distorted region with a thickness of about four atomic layers. Some steps in the stacking fault plane become also visible. The presence of Na has been further proven at a second TEM specimen of another individual stacking fault.

Obviously, Na atoms segregate along stacking faults when they reach the SiN_x/Si interface. In [4] an electrostatic hypothesis of the shunt mechanism was proposed. The present results require a different explanation. According to their high density alongside stacking faults, the Na atoms are supposed to create a band of states across the whole band gap. (At least implanted Na atoms as impurities on interstitial positions create donor states in Si crystal bulk material [8, 9].) In consequence, the stacking faults may become highly conductive. Due to the crossing of the p–n junction they appear as ohmic shunts.

The prementioned results and considerations are concluded in the following model, which differs in items (iv) and (v) from former proposals made in [3, 4]:

(i) A necessary prerequisite for PID is that a certain amount of charges is accumulated at the surface of the SiN_x ARC. In a module this is only possible if glass and encapsulants are conductive for mobile ions, e.g. Na, leading to leakage currents [2]. In corona charge experiments [10] these charges are applied directly to the SiN_x surface.

(ii) Charges (especially Na ions) at the ARC surface induce a strong field across the SiN_x layer, if its *electronic* conductivity is low enough [11].

(iii) Under the influence of this field, mobile Na ions, which penetrate from the surface or which are resident within the SiN_x layer are driven towards the SiN_x/Si interface. When the ions accumulate in the SiO_x interlayer, their positive ion charge prevents further Na drift to the interface.

(iv) The observed stacking faults predominantly provide extended diffusion channels into the Si crystal. (Thermal diffusion of Na in Si bulk is low at room temperature [9].) Stacking faults are heavily decorated by Na and thus become conductive. This process leads to

the observed shunting of the p–n junction. If the Na ions enter the stacking fault, their charges become neutralized, thereby enabling more Na to drift towards the SiN_x/Si interface.

(v) The reverse process (PID recovery) seems to be diffusion driven: Na diffuses back into the thin interfacial SiO_x layer. Further thermal back-diffusion into the SiN_x layer is delayed [12], leading to slow regeneration [13]. (Therefore, PID recovery can be accelerated with reverse potential across the SiN_x layer.) Dependent on the transport of Na ions back into the SiN_x layer, more Na is enabled to get out of the stacking faults. As Na is released from stacking faults, the conductivity throughout the p–n junction decreases. Hence the shunt resistance increases again.

The verification of the proposed model, especially regarding the mechanism of PID recovery, is already in progress and will be part of a future publication.

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