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GLUE-CLEAVE: KERFLESS WAFERING FOR SILICON WAFERS WITH METAL ON GLUEING AND REMOVABLE INTERFACE

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ABSTRACT

In literature different methods can be found to cleave silicon wafers or chips from the silicon block. These techniques are interesting for cost effective PV production, since they are kerf-less and material consumption for one wafer is at a minimum. In this paper a new method is proposed, which is based on mechanical loads in a layer system of silicon, glueing material, and a re-usable metal stripe. In its final stage, this method does not need to heat up and cool down the whole silicon crystal for each spalling cycle and thus may be considerably more time and energy efficient than previous thermal spalling methods. First experiments were successfully performed to thermally cleave (10x10) mm² silicon chips. By using analytical and numerical models, more insight in the fracture mechanical process was given and important material and geometry parameters were identified in order to optimize the process.

1 INTRODUCTION

In crystalline silicon photovoltaics the costs strongly depend on the material and manufacturing costs up to the wafer substrate for cell processing [1]. With decreasing prices for poly-silicon the crystallization costs can be reduced. But also in multi-wire wafering new technologies, as the diamond wire sawing, are assumed to reduce the manufacturing costs drastically by higher throughput and cutting thinner wafers [2]. In order to further decrease material consumption, new kerf-less wafering technologies have been developed, which can be applied after crystallization [3-6]. Besides [4], most of the techniques are based on the findings of Suo and Hutchinson [7] using the stress field in a brittle substrate beneath a thin layer of a different material. By using layer materials with according properties, residual stresses can be induced in the layer system and a crack propagates in the brittle substrate parallel to the interface due to the criteria $K_{II}=0$ and $K_I=K_{Ic}$, where K is the stress intensity factor of different loading conditions I, II, and III [8]. The distance of the crack to the interface, i.e. the thickness of the final substrate, depends on material properties and geometry of the layer system.

Often, thin layers of metal in combination with a temperature process are used for the cleavage on silicon substrates. Though, if it is necessary that the metal layer is removed after the cleaving process, subsequent process steps are needed. Thus, it would be interesting to fix the metal layer on silicon by using another material, which can be easily detached from the silicon wafer after cleavage and can be re-used again. Thus, the “Glue-Cleave” process was introduced by O. Breitenstein [9]. This technique covers the possibility to glue a metal layer on a silicon block and introduce a mechanical load to cleave a silicon wafer from the block (see Figure 1). This paper presents the Glue-Cleave process by using a silicon block, solder glass as glue and an Invar steel stripe. Furthermore, numerical investigations were performed to investigate the fracture mechanics, considering different possible material systems for this process.

2 MATERIALS AND METHODS

2.1 Experimental Setup and Samples

In Figure 1 the principle of Glue-Cleave, as well as the experimental setup, is shown. For the experiments, a monocrystalline silicon block of (10x10x10) mm³ with a {111} orientation on the top surface was used. Solder glass was chosen in order to investigate the use of a possible glueing and removable layer between silicon and the metal layer. In this analysis solder glass powder (type SCHOTT G018-223 K3) was molten on a metal stripe (Invar steel) by heating the metal by electricity using a high current transformer. The solder glass melts approximately at 400°C, while the glass transition point is in the range of 325°C. Invar steel was used as metal stripe (thickness of 300µm), because of lower CTE mismatch to silicon and similar Young's modulus. In the experiment the metal stripe was heated up until the solder glass became liquid. Then the silicon block was put on the liquid glass on the metal stripe. After cooling down to room temperature, it was supposed to extract a silicon layer by an external force at the metal layer. However, due to the temperature-induced stress in the silicon-metal sandwich the cleavage occurred spontaneously during cooling down. After cleavage and reheating, the solder glass became liquid again and the chip could be detached from the metal stripe.

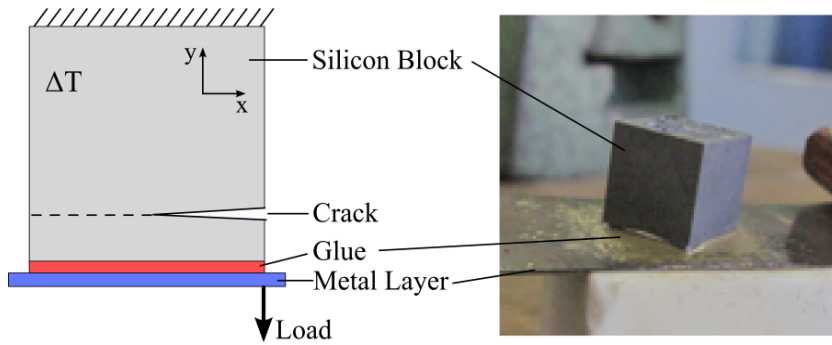


Figure 1: Principle of Glue-Cleave and experimental setup

2.2 Modeling

The modeling of the mechanical system was performed analytically, using equations of [7], as well as numerically. For numerical modeling, the layer system of metal, glue and silicon block the Finite-Element-Method (FEM) was used. In Figure 2 the 2-dimensional FE model is shown, which was used for numerical analysis within the Ansys FE code. Higher order 2-dimensional plane elements were used considering plane strain conditions, which represents a center cross section of the block. The boundary conditions were fixed in x and y direction on one side of the metal stripe and fixed in y direction on the other side of the stripe. Thus, the metal stripe can deform easily and it is close to the conditions in the experimental fixture (cf. Figure 1). The crack was modeled as a line of a defined length with unconnected elements. Crack tip elements were used at the crack tip to consider the asymptotic stress field and calculate the stress intensity factors K_I and K_{II} . Using the stress intensity factors, the energy release rate can be calculated for plane strain as [8]

$$G = \frac{E}{1 - \nu^2} (K_I^2 + K_{II}^2) \quad (1)$$

The criteria for crack growth, $K_I = K_{Ic}$ and/or $G = G_c$, requires material values for K_{Ic} and G_c . For silicon the values $K_{Ic} = 0.83 \text{ MPa m}^{1/2}$ and $G_c = 3.83 \text{ J/m}^2$ for the {111} plane were used in this analysis [10].

The load was applied by thermal uniform temperature difference of $\Delta T=300\text{K}$. Deformation and stresses are induced due to different thermal and mechanical properties of the layers. The material constants of the different materials used in this analysis are summarized in Table 1. All materials were considered as linear elastic isotropic materials.

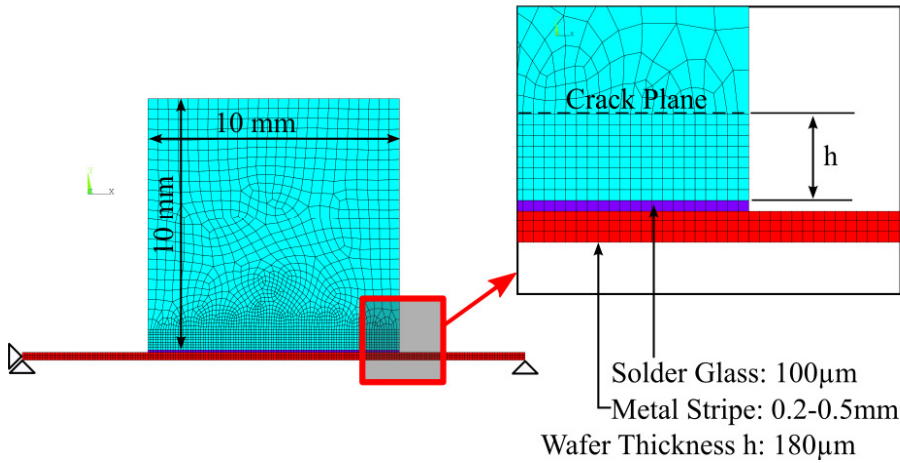


Figure 2: FE model of silicon block, solder glass and metal layer (stripe) with geometric parameters and boundary conditions.

Table 1: Material constants used for analytical and numerical analyses.

Material	Young's Modulus [GPa]	Poisson's Ratio [-]	Coefficient of Thermal Expansion CTE [$10^{-6}/\text{K}$]
Silicon (isotropic)	168	0.28	2.616
Solder Glass	70	0.25	3.0
Invar (sort of steel)	148	0.3	4.8
Steel	200	0.29	12.6
Copper	110	0.343	16.4
Ceramic (Al_2O_3)	300	0.25	5.0

3 RESULTS

3.1 Experimental Results

After performing different experiments, as described in section 2.1, one could mostly observe the clear thermo-mechanically induced cleavage of a chip from the small silicon block as shown in Figure 3.

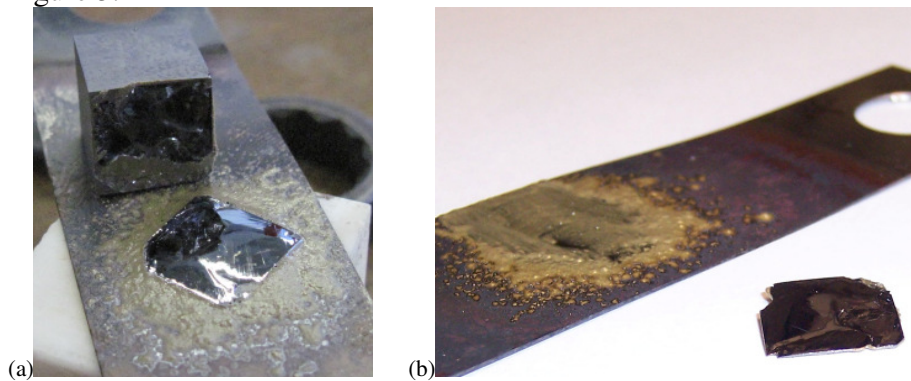


Figure 3: Cleaved silicon chip after performing Glue-Cleave experiment:
 (a) cleaved block with fixed silicon chip on solder glass and metal stripe
 (b) removed silicon chip after reheating

Actually, it was hoped that the silicon material would not spall spontaneously and the wafer could be spalled after cooling down by mechanical loading. However, while cooling, stresses were induced in the silicon block, which lead to spontaneous cleavage of a $(10 \times 10 \times 0.2)$ mm³ chip during cooling to room temperature. The thicknesses of the chips were in the range of 200 μ m. The fracture surface is mirror like, but the chip thickness is not homogeneous, as can be seen in Fig. 3a. The surface is produced by one propagating crack, which ran fairly straight through the material. In this setup the layer thickness of the solder glass was not optimized, which could also affect the thickness variation of the chips. For better understanding, and later hopefully preventing this spontaneous thermal spalling process, numerical investigations of the thermal spalling process on this silicon-glue-metal system were performed.

3.2 Numerical Results of Simulations

The simulations performed by the FE model introduced in Section 2.2 were concentrated on a final wafer thickness of 180 μ m. As an example, the displacement in y direction is shown in Figure 4 for different crack length simulations.

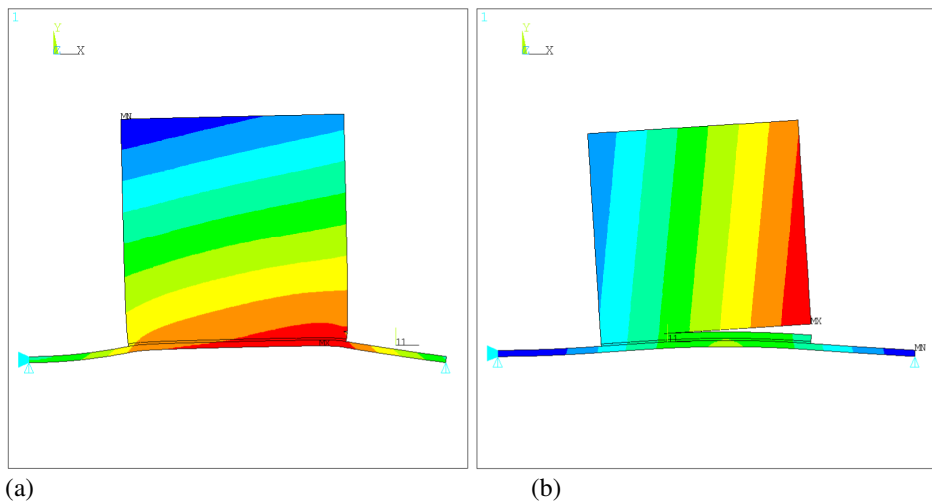


Figure 4: Results of displacement in y direction after different length of crack propagation: (a) 0.2mm (b) 7mm (thickness of metal layer: 300 μ m)

In Figure 5 detailed results for the energy release rate and the stress intensity factors are shown for different materials. As it can be seen, steel and copper as layer material show the highest energy release rate, which can be two orders of magnitude larger than the critical value for silicon.

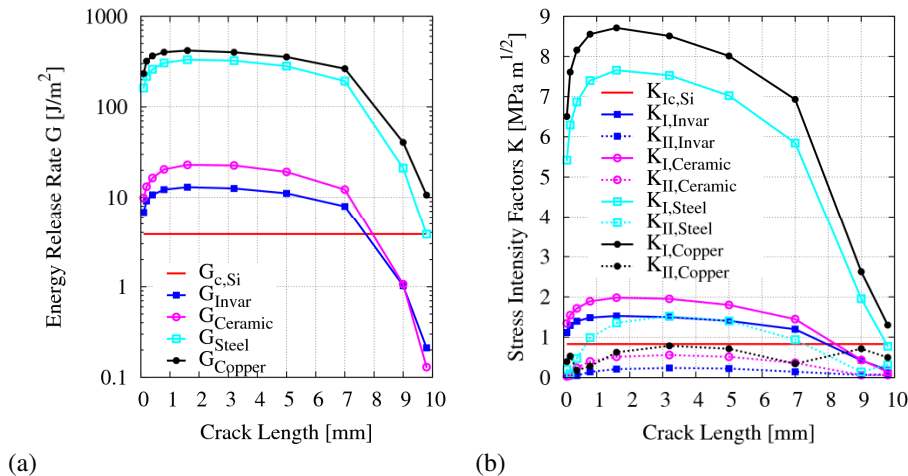


Figure 5: Results of (a) stress energy release rate (b) stress intensity factors for different materials and crack lengths (red line indicates critical values for silicon); thickness of metal layer: 300 μ m

If the crack is nearly as long as the block length, the energy release rate is decreasing strongly, since the elastic energy is very small in the system close before the full separation. For Invar and the ceramic material, the energy release rate is also much higher than G_c . Thus, crack propagation will occur. Though, for long cracks the energy release rate early drops below the critical value at 80-90% of the block length. That could cause uncleaved wafers on the block. Nevertheless, a lower stored energy could be appropriate for smooth crack planes. The high K_I values for all layer materials indicate that crack propagation is likely in the plane parallel to the interface. The relative value of K_{II} would be important to quantify the probability of kinking cracks. Interestingly, copper seems to have a much better ratio of K_I/K_{II} than steel for a similar energy release rate. That would mean that the crack in silicon will rather propagate in one plane when using copper compared to steel.

Besides different layer materials, one could also change the thickness of the metal or ceramic layer, which is glued on the silicon block by the solder glass. In Figure 6 the results for the energy release rate and the stress intensity factors are shown for different layer thicknesses of Invar steel, as used in the experiment. With increasing layer thickness, the energy release rate is also increasing, while the curves are not changing qualitatively. The values drop below G_c at nearly the same position in the silicon block. In comparison, the stress intensity factors show a similar behavior with increasing values for thicker layers. Though, the K_{II} values also increases and the ratios of K_I/K_{II} decreases for thicker layers, which could lead to a higher probability of kinking cracks for thicker layers. In correlation to the experiment, which is represented by $G_{300\mu m}$ in Figure 6, one can see that the system had enough energy for spontaneous spallation as seen in the experiment. Despite the use of solder glass with low melting temperature and Invar steel with smaller CTE, the silicon chip was cleaved by thermal induced stresses.

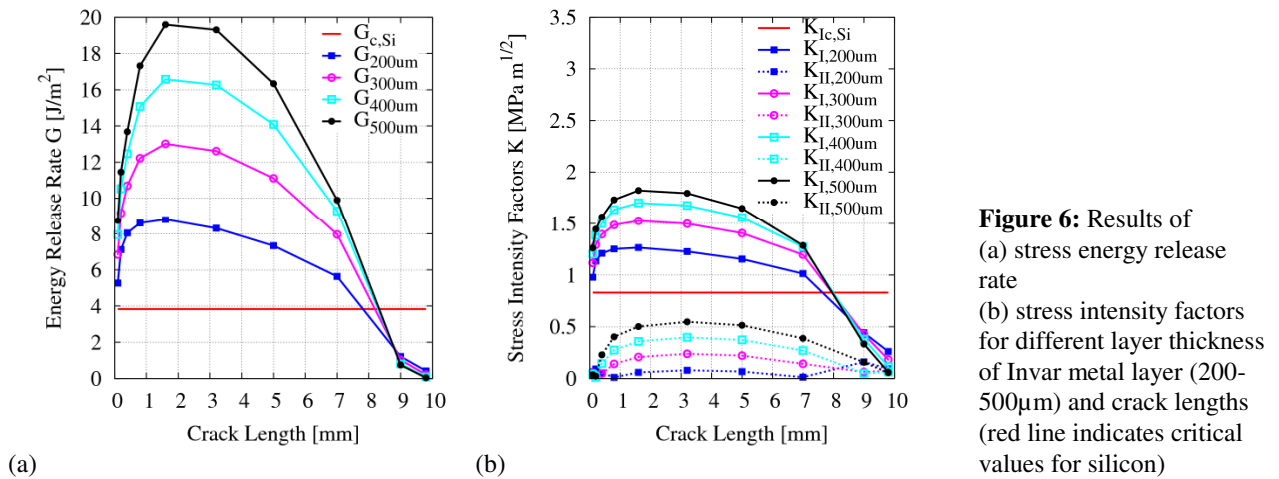


Figure 6: Results of (a) stress energy release rate (b) stress intensity factors for different layer thickness of Invar metal layer (200-500 μm) and crack lengths (red line indicates critical values for silicon)

Evaluating the equations following [7], which is not shown in this paper, one derives that the CTE has much more effect on the energy release rate and the stress intensity factors than the Young's modulus. Thus, it is preferable to choose materials with low CTE mismatch, if thermal spallation wants to be avoided. If there is a large mismatch, the stored energy for crack growth is large and the crack could branch and kink out or jump between cleavage planes, which would result in inhomogeneous thickness profiles. In conclusion, material properties and the geometry of the layer system with a glue component are important parameters to understand the crack propagation. With analytical and numerical models the cleavage process can be analyzed and optimized.

4 DISCUSSION

In this paper first principle experiments were performed for the Glue-Cleave process. The experiments showed interesting results on small scale (10x10) mm² and proof that spallation with a glueing and removable interface can work. The advantage of a melt glue would be that one can detach metal and silicon easily after the cleavage process by simply heating the sandwich, while the remaining glue at the metal stripe could even be re-used. Most importantly, if the wafer is cleaved by mechanical load via the metal stripe, large temperature variations are not necessary. Thus, for glueing the metal stripe to the bulk crystal not the whole crystal has to be heated up, but local heating may be sufficient. This means that, for this originally intended procedure with mechanical spalling, the bulk crystal may stay at an essentially constant temperature and needs not be heated up and cooled down with its whole volume for each single spalling cycle, as it is necessary for most other previous thermal spalling methods. This may considerably speed up the spalling process and save heating and cooling energy. In addition, small induced thermal stresses may even support the spalling procedure.

Obviously, if solder glass is used as a melt glue, even the use of Invar steel with lower CTE is not sufficient to prevent spontaneous thermal spalling. Besides solder glass, also other materials (e.g. polymers) could be used for the glueing interface. The requirements would be a good fixture for metal and silicon. It was recently shown by [11] that the fixture of epoxy is good enough to enable thermal spalling of silicon.

Based on simulation models the thermal spalling process was analyzed in more detail. In static analysis it was shown for the experimental data that the crack tends to stop 20% before reaching the end of the silicon block. In experiments this was not observed. Since the process is highly dynamic, also dynamic crack growth mechanisms need to be considered, which could force further crack propagation. Besides dynamic aspects, also the 3-dimensional crack front should be considered to quantify the crack propagation more precisely. Furthermore, considering the ratios K_I/K_{II} with respect to the anisotropic cleavage behavior of silicon could give even more insight. Nevertheless, the used simulation models are able to qualify the cleavage process and identify important material, geometry and process parameters. Based on this information material systems could be defined, which either reduce the thermally induced stress in silicon to a minimum or which are able to induce stress close to the critical values of G and K for silicon, but always stay smaller in order to prevent spontaneous cleavage. Together with small mechanical forces this combination could be used to initiate controlled cleavage.

5 CONCLUSION

Different methods may be found in literature to cleave silicon wafers or chips from the silicon block. These techniques are interesting for cost effective PV production, since they are kerf-less and material consumption for one wafer is at a minimum. Most of these methods are based on thermal stress between the silicon and an attached layer, which is usually not re-usable. In this paper a new method is proposed, which is based on mechanically introduced loads on a layer system of silicon, glueing material, and a re-usable metal stripe. In a first experiment solder glass was used as a glue and Invar steel as the metal. For this system spontaneous thermal spalling appeared. Since the first experiments were successfully performed to cleave (10x10) mm² silicon chips, this method seems to be a promising technique to cleave silicon wafers and to easily remove the required metal layer. Until now, only the spontaneous thermal spalling process in this system was modelled. Further modelling will be carried out for mechanically induced spalling. The FE models showed that they

can be used for detailed fracture mechanical analysis and investigations of important material and geometry parameters in order to optimize the process.

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REFERENCES

- [1] European Photovoltaic Technology Platform (2011): A Strategic Research Agenda for Photovoltaic Solar Energy Technology, European Union
- [2] International Technology Roadmap for Photovoltaics (ITRPV) (2012), SEMI PV Group
- [3] Dross, F.; Robbelein, J.; Vandeveld, B.; Van Kerschaver, E.; Gordon, I.; Beaucarne, G. & Poortmans, J. (2007): Stress-induced large-area lift-off of crystalline Si films. *Applied Physics A: Materials Science & Processing*, 89, 149-152
- [4] Henley, F.; Kang, S.; Liu, Z.; Tian, L.; Wang, J. & Chow, Y.-L. (2009): Beam-induced wafering technology for kerf-free thin PV manufacturing. In: 34th IEEE Photovoltaic Specialists Conference, 001718 -001723
- [5] Bedell, S. W.; Shahrjerdi, D.; Hekmatshoartabari, B.; Fogel, K.; Lauro, P.; Sosa, N. & Sadana, D. (2011): Kerf-Less Removal of Si, Ge and III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies. In: 37th IEEE Photovoltaic Specialists Conference
- [6] Rao, R. A.; Mathew, L.; Saha, S.; Smith, S.; Sarkar, D.; Garcia, R.; Stout, R.; Gurmu, A.; Onyegam, E.; Ahna, D.; Xu, D.; Jawarani, D.; Fossum, J. & Banerjee, S. (2011): A NOVEL LOW COST 25um THIN EXFOLIATED MONOCRYSTALLINE SI SOLAR CELL TECHNOLOGY. In: 37th IEEE Photovoltaic Specialists Conference
- [7] Suo, Z. & Hutchinson, J. W. (1989): Steady-state cracking in brittle substrates beneath adherent films. *International Journal of Solids and Structures*, 25, 1337-1353
- [8] Lawn, B. (1993): *Fracture of Brittle Solids*. Cambridge University Press
- [9] German patent DE 10 2010 013 549 A1, Breitenstein O. (2010): Method for fabricating wafers from volume material (in German: Verfahren zur Herstellung von Wafern aus Volumenmaterial)
- [10] Bagdahn, J. (2000): *Festigkeit und Lebensdauer direkt gebondeter Siliziumwafer unter mechanischer Belastung*. Phd Thesis, Martin-Luther-Universität Halle-Wittenberg
- [11] Martini, R.; Gonzalez, M.; Dross, F.; Masolin, A.; Vaes, J.; Frederickx, D. & Poortmans, J. (2012): Epoxy-induced spalling of silicon. *Energy Procedia/Silicon PV* (to be published)