CRYSTAL GROWTH & DESIGN

ARTICLE

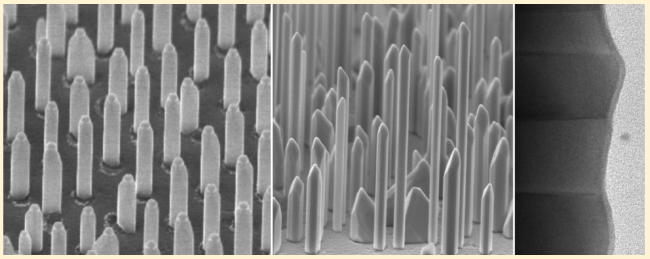
pubs.acs.org/crystal

Fabrication of High-Quality InSb Nanowire Arrays by Chemical Beam Epitaxy

Alexander T. Vogel,*[,†] Johannes de Boor,[†] Joerg V. Wittemann,[†] Samuel L. Mensah,[†] Peter Werner,[†] and Volker Schmidt[†]

[†]Max Planck Institute of Microstructure Physics, D 06120 Halle (Saale), Germany

ABSTRACT: We present investigations on InSb nanowires grown directly on InSb substrates. A chemical beam epitaxy system was used to synthesize InSb nanowires. Growth at low temperatures (300−400 °C) resulted in extensive parasitic InSb thin film deposition and stacking faults within these nanowires. To circumvent both problems, InSb nanowires were synthesized at temperatures above 410 °C. By further optimizing the growth parameters completely stacking fault-free, free-standing InSb nanowires were obtained. By combining chemical beam epitaxy and laser interference lithography, large areas of ordered InSb nanowires were fabricated. Temperature-dependent electrical measurements on these InSb nanowire arrays showed intrinsic bulklike behavior.



INTRODUCTION

Among all known semiconductors, bulk InSb has the highest electron mobility of 77000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, along with a sizable hole mobility of 850 $cm^2 \cdot V^{-1} \cdot s^{-1}$.[1,2] This makes InSb a promising candidate for high-speed, low-power electronics.[3] Besides, InSb has the largest lattice constant (a_0 = 0.648 nm) and the smallest band gap (0.17 eV) among the III−V semiconductors, with the latter qualifying InSb for IR emission and detection.[4] Moreover, InSb is an excellent candidate for spin-related and quantum-effect studies due to its large g-factor and the huge exciton Bohr radius of 60 nm.[5] Another outstanding property of InSb is its large thermoelectric figure-of-merit of 0.6, which furthermore increases with smaller feature sizes.[6,7]

In general, III−V materials crystallize in either the cubic zinc blende or the polytypic hexagonal wurtzite structure—or a combination of both.[8] These two structures are so similar that a stacking fault in one structure can be locally regarded as a very small segment of the respective other structure. Within the zinc blende phase, altering the stacking sequence can give rise to a twin plane, representing a mirror plane between two stacking fault-free segments.[9] Among arsenic and phosphorus based nanowires, it is rather uncommon to find nanowires consisting of the pure zinc blende phase. Due to the low ionicity of InSb (f_i = 0.19), the cubic zinc blende structure is much more stable (compared to arsenic and phosphorus based nanowires), and hence, the energy required to form a stacking fault and/or twin is substantial. For InSb the energy difference between the wurtzite and zinc blende structure was calculated to be 8.2 meV/atom. Only AlSb (9.5 meV/atom) and GaSb (9.9 meV/atom) show higher values.[10] This high energy difference favors the formation of stacking fault-free InSb nanowires, as will be demonstrated within this report.

However, controlled epitaxial growth of InSb nanowires is challenging due to its huge lattice mismatch with respect to common semiconductor substrates such as Si (19%), GaAs (15%), or InAs (7%), although by the use of low temperature buffer layers thin film growth of InSb has been demonstrated.[11] Furthermore, due to the low melting point of InSb (T_m = 525 °C) in combination with the rather high decomposition temperature of common antimony precursors,[12] the temperature window for InSb growth is rather small. As yet, only few reports on controlled epitaxial InSb nanowire growth exist,[13−16] and notably, these works have in common that severe parasitic thin film growth was observed.

Herein we report the synthesis of InSb nanowires grown on InSb$(-1-1-1)_B$ substrates using chemical beam epitaxy (CBE). CBE has some distinct advantages over other epitaxial growth techniques such as molecular beam epitaxy (MBE) and metal−organic vapor phase epitaxy (MOVPE). Compared to MBE, the growth rate is much higher and source control is easy due to the use of electronic mass flow controllers. In contrast to MOVPE, the accessible temperature window is significantly larger in CBE, as the Sb precursor is thermally precracked by a cracker cell.

We present a comparative study on InSb nanowire growth at low temperatures (300−400 °C) and high temperatures (>410 °C), respectively. To investigate the influence of temperature on nanowire growth, Au colloids dispersed on InSb substrates are used. By using substrates prestructured by laser interference lithography (LIL) and carefully optimizing the growth parameters, we managed to fabricate regular arrays of

Received: January 17, 2011
Revised: February 25, 2011
Published: March 21, 2011

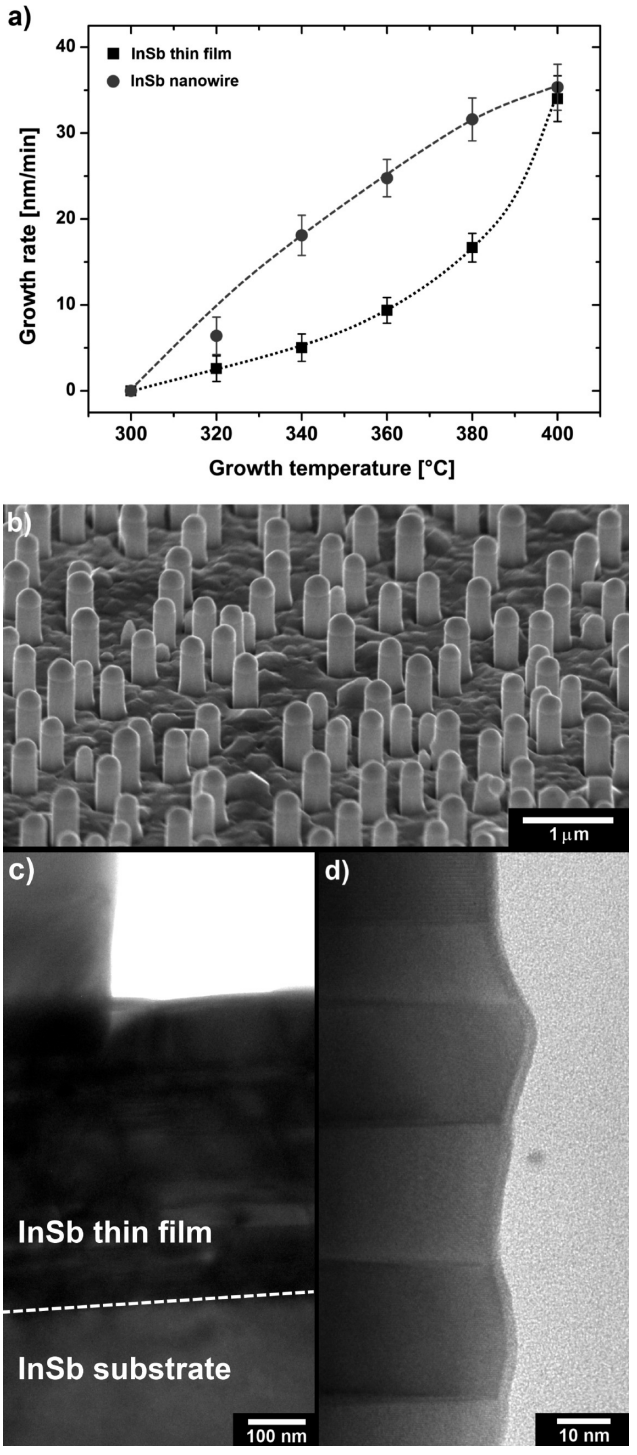


Figure 1. (a) Graph showing the growth rate dependence on the growth temperature for InSb nanowires and InSb thin film grown on InSb-$(-1-1-1)_B$ substrates (V/III = 2). (b) SEM image of InSb nanowires grown at 380 °C. (c and d) TEM and HRTEM image of these wires grown at 380 °C. The defect-rich InSb thin film can clearly be seen.

stacking fault-free InSb nanowires. These arrays are then employed for temperature-dependent electrical characterization.

EXPERIMENTAL SECTION

Using a noncommercial cold-wall CBE reactor, InSb nanowires are grown on "epi-ready" InSb$(-1-1-1)_B$ substrates (Firebird Technologies Inc.). Metal−organic (MO) precursors are directly injected into the growth chamber without the use of a carrier gas. Mass flow controllers (MKS Instruments) are used for precursor dosing and switching. The precursors are trimethylindium (TMIn, Akzo Nobel HPMO, Selected Semiconductor grade) and triethylantimony (TESb, Akzo Nobel HPMO, Selected Semiconductor grade). Because of the high dissociation energy of TESb and the absence of homogeneous decomposition due to the low process pressure, a thermal cracker cell is used to precrack TESb at a temperature of 625 °C. At that temperature, the cracking efficiency of TESb is nearly 1. This procedure provides mainly Sb_2 and Sb_4 molecules. The base pressure of the growth chamber is in the lower 10^{-8} mbar regime. During growth, the pressure rises to 10^{-5} to 10^{-4} mbar, depending on the actual precursor flux entering the growth chamber. The substrate temperature is obtained by calibrating the heater with respect to the substrate (using type k thermocouples). Additionally the temperature is cross-checked by using an optical pyrometer with a spectral response of 1.6 μm.

InSb substrates are rinsed in acetone and isopropanol prior to Au colloid deposition. For this aim, a sticking agent (poly-L-lysin, Sigma-Aldrich, 0.1% w/v aqueous solution) and then an Au colloid solution (BBI International) containing Au colloids with a diameter of 40 nm are spin coated onto the substrate's surface. Samples are then immediately loaded into the CBE system. Poly-L-lysin is not stable at temperatures above 180 °C and, therefore, readily evaporates while heating up to the desired growth temperatures.

Nanowires are characterized by means of scanning electron microscopy (SEM) using a JEOL JSM-6701F with an acceleration voltage of 3 kV. All SEM images are tilted by 60° toward the reader. Structural characterization is carried out by (HR)TEM using a JEOL JEM-4010 operated with an acceleration voltage of 400 kV. Electrical characterization is carried out using a noncommercial cooling stage and Keithley measurement equipment.

RESULTS AND DISCUSSION

Figure 1a shows the relationship between the growth temperature and the InSb nanowire growth rate. Growth temperatures range from 300 to 400 °C. The TMIn flux is fixed at 0.17 sccm, and the V/III ratio is set to be 2. Additionally, a parasitic InSb thin film forms, embedding parts of the InSb nanowires. The growth rate dependence of the thin film on the growth temperature is also shown in Figure 1a. The nanowire growth rate is calculated by dividing the total nanowire length (embedded and free-standing part) by the growth time. The error bars originate from the deviation in nanowire length because of the growth rate dependence on the nanowire diameter, which may differ from one wire to another. No InSb growth (both thin film and nanowires) is observed at temperatures below 320 °C. We attribute this to the limited decomposition of TMIn, which only starts at around 300 °C.[17] With increasing growth temperature, the formation of the parasitic thin film becomes even more pronounced. At a temperature of 400 °C, the ratio of nanowire growth rate to thin film growth rate is nearly 1. The longest freestanding InSb nanowire segments were grown at 340 and 360 °C. At these temperatures, the ratio of nanowire to thin film growth rate amounts to 3.6 and 2.9, respectively.

From the data presented in Figure 1a, we obtain an activation energy of 0.69 eV for InSb thin film growth. This value is reasonably close to the value of 0.94 eV given by Persson et al.[18] for TMIn decomposition on InAs$(-1-1-1)$B substrates.

Figure 1b shows a SEM image of InSb nanowires grown at 380 °C. All nanowires grow perpendicular to the substrates surface along the $[-1-1-1]$ direction. The thick InSb thin film

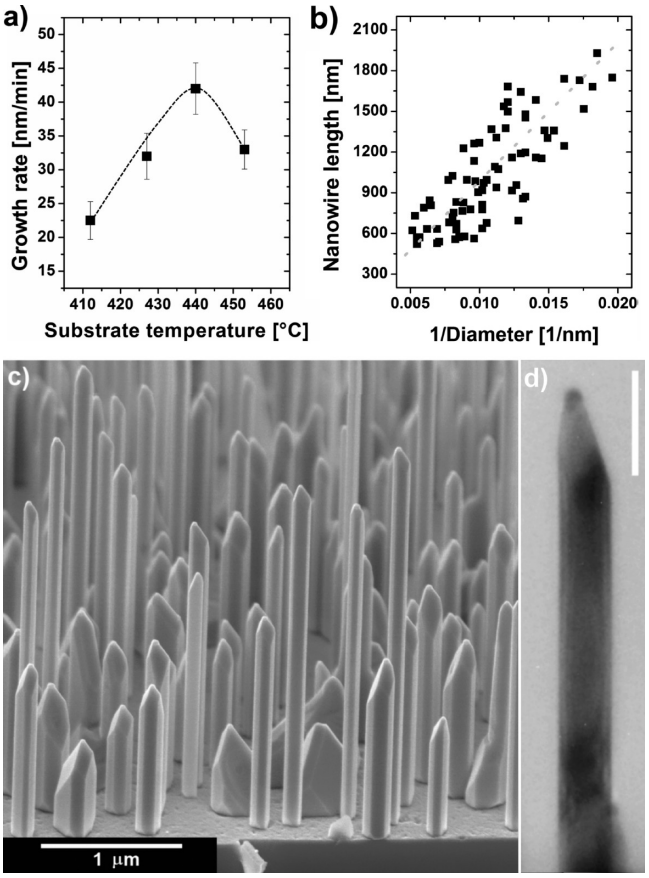


Figure 2. (a) Growth rate dependence on the growth temperature for InSb nanowires grown at growth temperatures higer than 400 °C (V/III = 15). (b) Nanowire length over the inverse nanowire radius for a sample grown at 450 °C and V/III = 15. (c) Corresponding SEM image. (d) Bright-field TEM image (along the [110] zone axis) of a stacking fault-free InSb nanowire. The scale bar corresponds to 100 nm.

embedding the lower parts of the nanowires is clearly visible. Note also, that the diameter (average ∼140 nm) increased heavily compared to the original Au particle diameter (40 nm). Comparing the initial Au volume to the volume of the seed particle after growth shows that the composition of the particle would correspond to an Au−In alloy with approximately 3 atom % Au. This is similar to what has been reported using Ag seed particles to grow InSb nanowires.[13]

Figure 1c shows a TEM image (zone axis parallel to the [110] direction) of a nanowire grown under the same conditions as those mentioned above (growth temperature = 380 °C, V/III ratio = 2). Again, the defect-rich parasitic thin film embedding the nanowire is clearly visible. Also, idiomorphic twinning parallel to the [−1−1−1] growth direction of the nanowire occurs. Figure 1d shows a HRTEM image of the twinned part of the nanowire. The twin boundaries are atomically sharp, and each segment is about 20 nm high. Idiomorphic twinning was described in phosphide and arsenide based nanowires[19] but has not been observed in InSb yet.

At temperatures between 320 and 400 °C, InSb nanowires growth using Au seed particles resulted in the formation of defect-rich InSb nanowires and/or the formation a thick InSb thin film embedding the nanowires. Since the stacking fault density inside the nanowires can be reduced by increasing the growth temperature,[13] nanowires are also synthesized at temperatures above 410 °C. At such high growth temperatures, nanowire formation behaves quite differently. For example, nanowires do not form at V/III ratios lower than 6. Figure 2a shows the dependence of nanowire growth rate on the growth temperature for wires grown with a V/III ratio fixed to 15. Again, the growth rate is calculated by dividing the measured nanowire length by the growth time. All samples are cooled in an Sb-rich atmosphere to prevent degradation of the grown structures while cooling down to room temperature. For these conditions, a growth rate maximum was reached at a growth temperature of about 440 °C. At temperatures above 440 °C, desorption of TMIn (and its pyrolysis products) becomes more and more pronounced, leading to a decrease of the nanowire growth rate. Note that this temperature is already quite close to what has been reported as the optimal growth temperature (460 °C) for InSb thin films.[20] Typically, (as a rule of thumb) the ideal temperatures for III−V nanowire growth are more than 100 K lower than the ideal temperatures for the corresponding thin films.[21,22] This does not seem to be the case for InSb.

Figure 2b shows a graph of nanowire length versus one over nanowire diameter for nanowires grown at 450 °C and with a V/III ratio set to 20. The solid line indicates a fit proportional to 1/diameter. This kind of dependence was previously observed and theoretically described for growth techniques relying heavily on surface diffusion processes.[23,24] Applying the model presented by Fröberg et al.,[25] we obtain an In-species diffusion length of about 350 nm on the InSb$(-1-1-1)_B$ surface.

Figure 2c shows a SEM image of nanowires grown at 450 °C and a V/III ratio of 20. All nanowires exhibit perfectly flat {110} side facets. Furthermore, we want to stress the point that, by applying these conditions, no parasitic InSb thin film forms, as we believe that this is a highly important outcome. Additionally, we investigated at least 50 nanowires in TEM and found no stacking faults. All TEM images (bright field and high-resolution mode) are taken along the [110] zone axis. One example is shown in Figure 2d. This is consistent with recent reports covering InSb nanowire growth at temperatures above 410 °C in MOVPE and CBE.[15−17] At this point we assume that, at least in CBE, nanowire growth takes place via a "surface-selective" growth mechanism. Due to the high V/III ratios used, a site blocking effect caused by excess Sb[26,27] prevents the formation of a parasitic InSb thin film. Nanowire growth only takes place where the seed particles preserve the pristine InSb$(-1-1-1)_B$ surface. Furthermore, the formation of stable {110} side-facets is favored by a high V−III ratio and growth temperature.[28,29]

For nanowires grown at temperatures higher than 411 °C, the seed particle located at the tip of the nanowires is identified to be $AuIn_2$ using HRTEM and X-ray diffraction. This alloy is of cubic FM-3M structure and is basically lattice matched to InSb. According to the ternary Au−In−Sb phase diagram, $AuIn_2$ may start to form at temperatures of around 400 °C. Considering our experimental results and the eutectic temperatures of the two known pseudobinary systems AuIn−InSb (T_E = 417 °C) and $AuIn_2$−InSb (T_E = 472 °C) within the ternary Au−In−Sb phase diagram, we are not able to conclude whether the seed particle is in liquid or solid state during growth.

When contacting a large number of nanowires using a macroscopic contact, one needs to have the ability to estimate the number of nanowires contacted. Therefore, we combined laser interference lithography and chemical beam epitaxy to grow ordered arrays of InSb nanowires directly on InSb$(-1-1-1)_B$

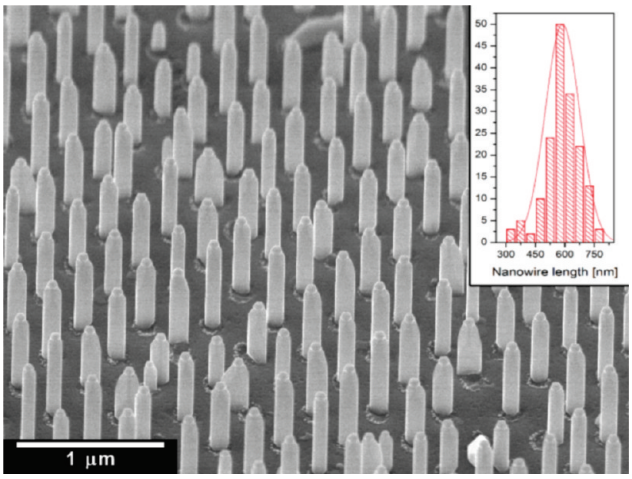


Figure 3. SEM image of an ordered InSb nanowire array obtained by combining laser interference lithography and CBE. The sample was grown at 411 °C and a V/III ratio of 20. The inset shows a histogram of the length distribution of those wires grown.

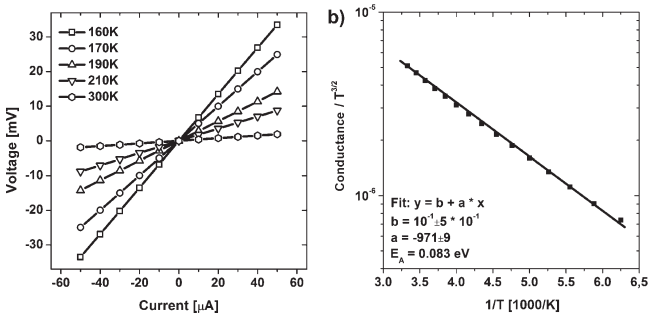


Figure 4. (a) Selected $I-V$ curves for temperatures between 160 K and 300 K measured on a InSb nanowire array. (b) Conductance/$T^{3/2}$ (to account for the $T^{3/2}$ term coming from the expression for the carrier density of states) of the contacted InSb nanowire array over 1/temperature.

substrates. In order to fabricate these arrays, a UV photoresist is spin coated onto the cleaned substrates and exposed by UV laser interference, which after photoresist development led to a hexagonal hole array.[13,30,31] By Au evaporation and liftoff, a hexagonal array of Au islands (diameter 120 nm, center to center distance 380 nm) is created. The advantage of laser interference lithography is that large area structuring is simple and fast.

Figure 3 shows a SEM image of InSb nanowires grown at 410 °C and a V/III ratio of 20. The pattern is homogeneous on a micrometer scale with about 95% of the wires growing at the predefined position. The filling factor is calculated to be about 5%. Shown in the inset of Figure 3 is the histogram of the length distribution of nanowires within that array. The standard deviation of the nanowire length is about 12%. We attribute this deviation to the growth rate dependence on the nanowire diameter since the diameter of the initial Au particle might vary and/or radial growth on the side facets might occur.

For temperature dependent electrical characterization, one of these arrays (using a larger wire-to-wire distance compared to the array shown above) was embedded in about 800 nm of polyimide (Sigma Aldrich). The polyimide covering the top of each wire is, in a second step, removed by oxygen plasma etching. Electrical contacts (area 1 mm^2) were achieved by evaporating Cr (3 nm) and Au (50 nm), contacting approximately 10^4 wires at a time. The backside of the InSb substrate is also contacted by Cr and Au. The sample is then mounted on a liquid nitrogen cooled sample holder and the $I-V$ characteristics is measured for temperatures between 160 K and 300 K.

The $I-V$ characteristics (Figure 4) clearly show linear behavior, suggesting ohmic contacts. From a logarithmic plot of the resistance as a function of the inverse temperature (see Figure 4 b), we extract an activation energy E_A = 0.083 eV. This matches half the InSb band gap of 0.17 eV. An activation energy of half the band gap is what one would expect for intrinsic charge carriers. Furthermore, since the activation energy resembles the value of InSb down to a temperature of 160 K, the intrinsic charge carrier concentration sets an upper limit for unwanted impurities/doping of 1×10^{14}.[32] Considering the geometry and number of nanowires, we extract a resistivity of ρ = 0.3 Ω·cm which is higher than the bulk resistivity ($\rho = 4 \times 10^{-3}$ Ω·cm). An increased resistivity was also measured by Caroff et al.[14] This is most likely due to a significantly reduced electron mobility caused by scattering at the nanowire surface.

In summary, we present growth investigations of InSb nanowires grown directly on InSb(−1−1−1)$_B$ substrates. Samples grown at low growth temperatures show extensive parasitic thin film growth and/or a large number of planar defects inside the InSb nanowires. To circumvent both problems, InSb nanowires are synthesized at temperatures above 410 °C. By optimizing all growth parameters, the parasitic thin film growth is eliminated and stacking fault-free InSb nanowires are grown. By combining chemical beam epitaxy and laser interference lithography, large areas of ordered InSb nanowire arrays are fabricated. These arrays are used for temperature-dependent electrical characterization. Those nanowires show good electrical conductivity but still had a resistivity 2 orders of magnitude higher than expected.

AUTHOR INFORMATION

Corresponding Author

*E-mail: avogel@mpi-halle.mpg.de. Phone: +49 345 5582 979. Fax: +49 345 5511 223. http://www.mpi-halle.mpg.de.

ACKNOWLEDGMENT

We want to thank Prof. Georg Schmidt (MLU Halle-Wittenberg) and Dr. Stephan Senz for helpful discussions. We also want to thank Mrs. Hopfe for TEM sample preparation. The financial support by the NanoSTRESS project is gratefully acknowledged. Above all, we would like to express our deep gratitude to Prof. U. Gösele (deceased November 2009) for all the relentless support and encouragement.

REFERENCES

(1) Riikonen, J.; Toumi, T.; Lankinen, A.; Sormunen, J.; Säynätjoki, A.; Knuuttila, L.; Lipsanen, H.; McNally, P. J.; O'Reilly, l.; Danilewsky, A.; Sipilä, H.; Vaijärvi, H.; Lumb, D.; Owens, A. *J. Mater. Sci.: Mater. Electron.* **2005**, *16*, 449–453.

(2) Heyns, M.; Tsai, W. *MRS Bull.* **2009**, *34*, 485–492.

(3) Ashley, T.; Barnes, A. R.; Buckle, L.; Dean, A. B.; Emeny, M. T.; Fearn, M.; Hayes, D. G.; Hilton, K. P.; Jefferies, R.; Martin, T.; Nash, K. J.; Philips, T. J.; Tang, W. H. A.; Wilding, P. J.; Chau, R. *7th Int. Conf. Solid-State Integrated Circuits Technol. Proc.* 2004, *3*, 2253−2256.

(4) Rogalski, A. *Prog. Quantum Electron.* **2003**, *27*, 59–210.

(5) Nilsson, H. A.; Caroff, P.; Thelander, C.; Larsson, M.; Wagner, J. B.; Wernersson, L.-E.; Samuelson, L.; Xu, H. Q. *Nano Lett.* **2009**, *9*, 3151–3156.
(6) Mingo, N. *Appl. Phys. Lett.* **2004**, *84*, 2652–26544.
(7) Mingo, N. *Appl. Phys. Lett.* **2006**, *88*, 149902.
(8) Algra, R. E.; Verheijen, M. A.; Borgström, M. T.; Feiner, L.-F.; Immink, G.; van Enckevort, W. J. P.; Vlieg, E.; Bakkers, E. P. A. M. *Nature* **2008**, *456*, 369.
(9) Caroff, P.; Dick, K. A.; Johansson, J.; Messing, M. E.; Deppert, K.; Samuelson, L. *Nature Nanotechnol.* **2009**, *4*, 50–55.
(10) Akiyama, T.; Sano, K.; Nakamura, K.; Ito, T. *Jpn. J. Appl. Phys.* **2006**, *45*, L275–L278.
(11) Service, R. F. *Science* **2009**, *323*, 1000–1002.
(12) Buchan, N. I.; Larsen, C. A.; Stringfellow, G. B. *J. Cryst. Growth* **1988**, *92*, 591–604.
(13) Vogel, A. T.; de Boor, J.; Becker, M.; Wittemann, J. V.; Mensah, S. L.; Werner, P.; Schmidt, V. *Nanotechnology* **2011**, *22*, 015605.
(14) Caroff, P.; Wagner, J. B.; Dick, K. A.; Nilsson, H. A.; Jeppsson, M.; Deppert, K.; Samuelson, L.; Wallenberg, L. R.; Wernersson *Small* **2008**, *4*, 878–882.
(15) Caroff, P.; Messing, M. E.; Borg, B. M.; Dick, K. A.; Deppert, K.; Wernersson, L.-E. *Nanotechnology* **2009**, *20*, 495606–495612.
(16) Ercolani, D.; Rossi, F.; Li, A.; Roddaro, S.; Grillo, V.; Salviati, G.; Beltram, F.; Sorba, L. *Nanotechnology* **2009**, *20*, 505605–505610.
(17) Fan, G. H.; Hoare, R. D.; Pemble, M. E.; Povey, I. M.; Taylor, G.; Williams, J. O. *J. Cryst. Growth* **1992**, *124*, 49–55.
(18) Persson, A. I.; Fröberg, L. E.; Jeppsen, S.; Björk, M. T.; Samuelson, L. *J. Appl. Phys.* **2007**, *101*, 034313.
(19) Dick, K. A.; Caroff, P.; Bolinsson, J.; Messing, M. E.; Johansson, J.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. *Semicond. Sci. Technol.* **2010**, *25*, 024009.
(20) Debnath, M. C.; Zhang, T.; Roberts, C.; Cohen, L. F.; Stradling, R. A. *J. Cryst. Growth* **2004**, *267*, 17–21.
(21) Dick, K. A. *Prog. Cryst. Growth Charact. Mater.* **2008**, *54*, 138–173.
(22) Bauer, J.; Gottschalch, V.; Paetzelt, H.; Wagner, G.; Fuhrmann, B.; Leipner, H. S. *J. Cryst. Growth* **2007**, *298*, 625–630.
(23) Jensen, L. E.; Björk, M. T.; Jeppesen, S.; Persson, A. I.; Ohlsson, J. B.; Samuelson, L. *Nano Lett.* **2004**, *4*, 1961.
(24) Zakharov, N.; Werner, P.; Sokolov, L.; Goesele, U. *Physica E* **2007**, *37*, 148–152.
(25) Fröberg, L. E.; Seifert, W.; Johansson, J. *Phys. Rev. B* **2007**, *76*, 153401.
(26) Noreika, A. J.; Francombe, M. H.; Wood, C. E. C. *J. Appl. Phys.* **1981**, *52*, 7416–7420.
(27) Asahi, H.; Kaneko, T.; Okuno, Y.; Itani, Y.; Asami, K.; Gonda, S. *J. Cryst. Growth* **1992**, *120*, 252–260.
(28) Bauer, J.; Paetzelt, H.; Gottschalch, V.; Wagner, G. *Phys. Status Solidi B* **2010**, *247*, 1294–1309.
(29) Noborisaka, J.; Motohisa, J.; Fukui, T. *Appl. Phys. Lett.* **2005**, *86*, 213102.
(30) de Boor, J.; Geyer, N.; Goesele, U.; Schmidt, V. *Opt. Lett.* **2009**, *34*, 1783–1785.
(31) de Boor, J.; Geyer, N.; Wittemann, J. V.; Goesele, U.; Schmidt, V. *Nanotechnology* **2010**, *21*, 095302.
(32) Oszwaldowski, M.; Zimpel, M. *J. Phys. Chem. Solids* **1988**, *49*, 1179–1185.